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DANA™

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INSTRUCTION MANUAL

980240

PRELIMINARY ISSUE

MODEL 2820

DATA AMPLIFIER

August, 1967

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Dana Model 2820 (Figure 1.1) is a direct-coupled, active guard differential amplifier with low noise at gains up to 12500, wide bandwidth, a high level of common mode rejection, and fast settling time. Full scale output is ±10 volts and 100mA.

The Model 2820 provides complete isolation between the two input leads and output common. The input, output, and power supply contain RF interference suppression from external RF noise. No common mode return path is required to achieve a common mode rejection of 120 dB, dc to 60 Hz.

Figure 1.1 - Dana Model 2820 Data Amplifier

Fail-safe circuits within the amplifier prevent damage from short circuits and from fault voltages up to 60 volts common mode (250 volts on low gain settings) and 30 volts normal mode. Overload recovery is 2 milliseconds from 500% overload of any duration. The step-function settling time is 500 microseconds.

System noise contributed by the amplifier circuitry is exceptionally low. The noise referred to the input at a gain of 1000 is less than 4 microvolts rms at full bandwidth and less than 1 microvolt, peak-to-peak, at a 10Hz bandwidth.

1.2 OPERATIONAL DESCRIPTION

A block diagram of the Model 2820 is shown in Figure 1.2. The Input Amplifier contains a Normal Mode Amplifier (NMA) and a Common Mode Amplifier (CMA). The NMA is a differential amplifier that amplifies the differential input voltage. Common mode voltage is effectively "cancelled out" in the NMA by feedback from the CMA. The CMA does this by sensing the common mode component of the signal in the first stage of the NMA and supplying an opposing voltage. The Output Amplifier consists of direct-coupled circuitry that determines the output characteristics of the amplifier. A portion of the output signal is applied back to the NMA through a precision attenuator network as negative feedback to define the closed-loop characteristics of the instrument. Amplifier gain is set by a voltage divider in the feedback network. Precision resistors are switched into this circuit by the GAIN switch. A detailed circuit description is given in Section 4.

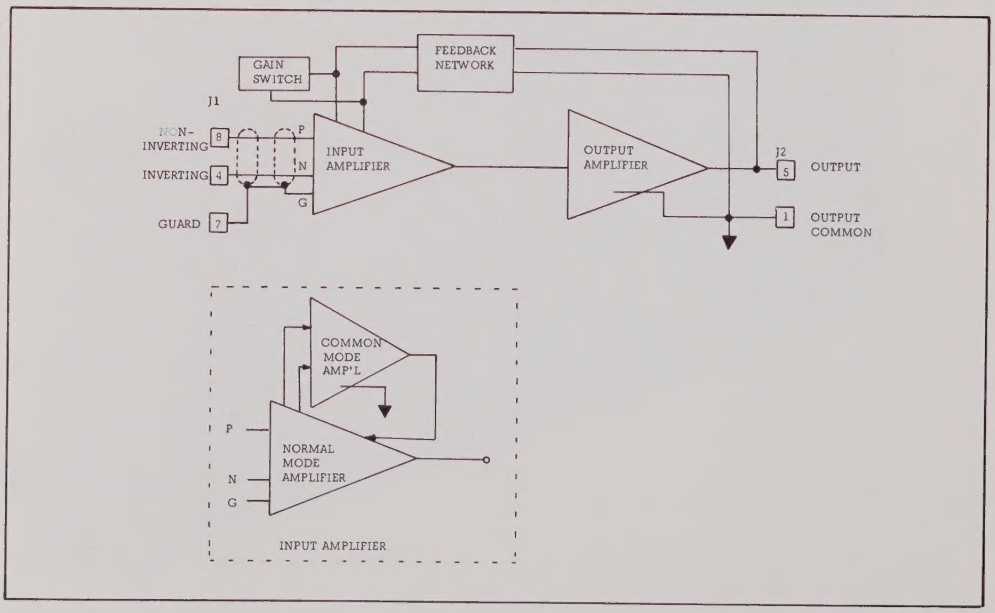


Figure 1.2 - Block Diagram, Model 2820

1.3 GAIN OPTIONS

Three gain options are available for various applications and must be specified when ordering the amplifier. They are designated as gain options V1, V2, and V3.

1.3.1 Option V1

The V1 option provides gain steps of 20, 50, 100, 200, 500, and 1000. A vernier multiplier extends each gain by a factor of 2.5:1. This feature allows continuous selection of gain values over the range of 20 to 2500. The V1 option is especially suited for use in applications where low-level, millivolt signals are to be amplified to voltage levels for accurate recording or measuring.

1.3.2 Option V2

The V2 option provides the same gain steps as the V1 option. Option V2, however, includes an X1/X.01 multiplier switch. This feature allows continuous selection of gain values over the range of 0.2 to 2500. The V2 option is especially suited for applications in which the input signal is already at a level of 1 volt or greater, or where the input may vary over a dynamic range from millivolts to full volts. Discriminators, potentiometers, and transformers are typical signal sources of this type and the amplifier serves as an isolation as well as scaling device.

1.3.3 Option V3

The V3 option provides gain steps of 100, 200,500, 1000, 2000, and 5000. A vernier multiplier extends each gain by a factor of 2.5:1. This feature allows continuous selection of gain values from 100 to 12,500. The V3 option is especially suited for applications that require an exceptionally high level of amplification such as a thermocouple temperature measuring system.

1.4 SPECIFICATIONS

Specifications are listed in Table 1.1. For definitions and a discussion of terms used refer to Appendix A, "Operating Characteristics and Definitions". Also, see "Low-Gain Considerations", paragraph 1.5.

1.5 LOW-GAIN CONSIDERATIONS

For easier evaluation of accuracy at low-gain operation, pertinent specifications are tabulated in Table 1.2 — in terms of percentage of full scale.

Table 1.1 - Specifications

DANA MODEL 2820 SPECIFICATIONS

A specifications apply for 0 to 350 ohm sources, in any unbalance.

Gain Option	Range	Steps	Accuracy	Resolution	Stability(at gain setting and constant temperature)	Temperature Coefficient
V1	20 to 2500 with 2.5:1 vernier	20,50,100,200, 500,1000	±0.1%	±0.01% (±0.1% worst case)	±0.01% (200 hours)	±0.005%/°C
V2	0.2 to 2500 with 2.5:1 vernier	0.2,0.5,1,2,5, 10,20,50,100, 200,500,1000	±0.1%	±0.01%(±0.1% worst case)	±0.01% (200 hours)	±0.005%/°C
V3	100 to 12,500 with 2.5:1 vernier	100,200,500, 1000,2000,5000	±0.1% K≤1000, ±0.15% K>1000	±0.01%(±0.1% worst case)	±0.01% (200 hours) K≤1000; ±0.01% x K/1000 (200 hours) K>1000	±0.005%/°C

	Gain (K) 20 to 1000	Gain (K) over 1000	Gain (K) below 20
OUTPUT (no damage for sustained short circuit)			
Full scale voltage	±10V	±10V	±10V
Voltage overrange, nominal	20%	20%	20%
Full scale load current	±100mA	±100mA	±100mA
Maximum short circuit current	±150mA	±150mA	±150mA
Impedance	0.1 ohm in series with 150uH	0.1 ohm in series with 150uH	0.1 ohm in series with 150uH
Capacitive load, without instability	0.33uF	0.33uF	0.33uF
Capability	Full scale voltage and current to 20kHz	Full scale voltage and current to 10kHz	Full scale voltage and current to 10kHz
FREQUENCY RESPONSE (at full output)			
Wideband dc to 100Hz	±0.01%	±0.02%	±0.01%
Minimum 3dB frequency	20kHz	10kHz	10kHz
Linearity (dc to 2kHz)	±0.01%	$\pm 0.005\% \times \frac{K}{100}$	±0.01%
COMMON MODE			
Rejection ratio dc to 60Hz	120dB, K = 1000 60dB + K in dB for all other gains	120dB, any gain	60dB, K = 10 40dB + K in dB for all other gains
Operating voltage dc to 60Hz	10V dc or peak ac	10V dc or peak ac	10V dc or peak ac
Fault voltage dc to 60Hz without damage	60V dc or peak ac	60V dc or peak ac	60V dc or peak ac
NOISE			
Full bandwidth	2uV rms RTI +2mV rms RTO	2uV rms RTI +2mV rms RTO	5mV rms RTO, any gain
10Hz	1mV peak to peak RTO, any gain	1mV peak to peak RTO, any gain	5mV peak to peak RTO, any gain
INPUT IMPEDANCE			
Normal mode	10Megohm, parallel with 0.002uF	10Megohm, parallel with 0.002uF	1Megohm, parallel with 0.002uF
ZERO STABILITY			
At constant temperature (after 30 minute warm-up)	±0.02% (200 hrs)	$\pm 0.02\% \times \frac{K}{1000}$ (200 hrs)	±0.1% (40 hours)
Temperature coefficient	(±0.001% RTO ±1uV RTI)/°C	(±0.001% RTO ±1uV RTI)/°C	(±0.001% RTO ±500uV RTI)/°C
STEP FUNCTION RESPONSE			
Settles to final value ±0.1% of full scale in	500 usec	1 msec	500 usec
Overload Recovery (to final value ±0.1% of full scale ±10uV RTI) 5 times full scale input, no damage for 30V dc or peak ac input on any gain	2 msec	2 msec	2 msec
TEMPERATURE RANGE (all options			
Operating	0°C to + 50°C		
Storage	-20°C to + 75°C		
POWER REQUIREMENT (all options)			
Domestic	105 to 125V rms, 50 to 400Hz, 6 watts		
Export Option 1	200 to 240V rms, 50 to 400Hz, 6 watts		
Export Option 2	215 to 265V rms, 50 to 400Hz, 6 watts		
Export Option 3	90 to 110V rms, 50 to 400Hz, 6 watts		

Table 1.2

Gain Setting	Zero Drift/Degree C as % of Full Scale	Error/Volt (Common Mode) as % of Full Scale
1000	0.011%	0.01%
500	0.006	0.01
200	0.003	0.01
100	0.003	0.01
50	0.002	0.01
20	0.001	0.01
10	0.051	0.05
5	0.026	0.05
2	0.021	0.05
1	0.011	0.05
0.5	0.006	0.05
0.2	0.003	0.05

1.6 AMPLIFIER ENCLOSURES

The Model 2808 Enclosure accommodates eight amplifiers. The enclosure is 7 inches in height with a depth of 22 inches and a width, including flanges, of 19 inches. The basic model is modified by a "dash" number which specifies the type of wiring interface.

The 2808 Enclosure accommodates all of the Dana Series 2800 Amplifiers. The amplifiers are interchangeable in the enclosure without alteration of the input and output cables.

The -1 Enclosure contains connectors to accommodate system wiring. Fusing and AC wiring are factory wired. A dimensional outline drawing (452402) of the 2808-1 Enclosure is included in Section 7, Drawings and Parts Lists.

The -2 Enclosure is fully wired. The inputs and outputs are accessible through connectors mounted on the rear panel. An outline drawing (452403) is included in Section 7, Drawings and Parts Lists.

1.7 AMPLIFIER ACCESSORIES

An Adapter Set Model 2801 (Dana part number 402468) and an Amplifier Support Bracket (Dana part number 452411) are used when the amplifier is operated on the bench. The Adapter Set (item 1 in Figure 1.3) contains input leads, output leads, and the power cord. The Amplifier Support Bracket (item 2 in Figure 1.3) mounts to the amplifier to support the amplifier in an upright position.

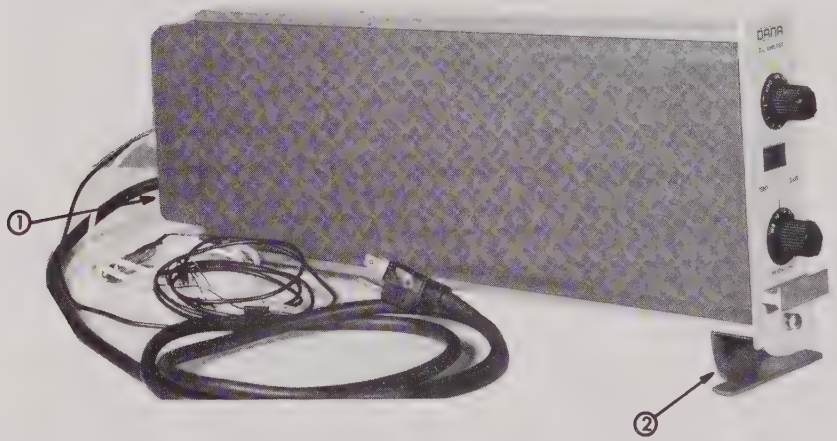


Figure 1.3 - Amplifier Accessories

SECTION 2

INSTALLATION AND INITIAL CHECKOUT

2.1 UNPACKING AND INSPECTION

The Dana Amplifier is shipped in a special reusable shipping package, designed to protect the instrument from excessive shock and vibration. Examine the package for signs of external damage before removing the unit. If external damage is present, notify the carrier before proceeding. Next, examine the outside of the amplifier for any evidence of damage due to excessive shock, vibration, water leakage, etc.

If the unit appears in perfect condition, proceed with the installation. However, if there is any apparent damage, communicate with the carrier for instructions.

2.2 POWER REQUIREMENTS

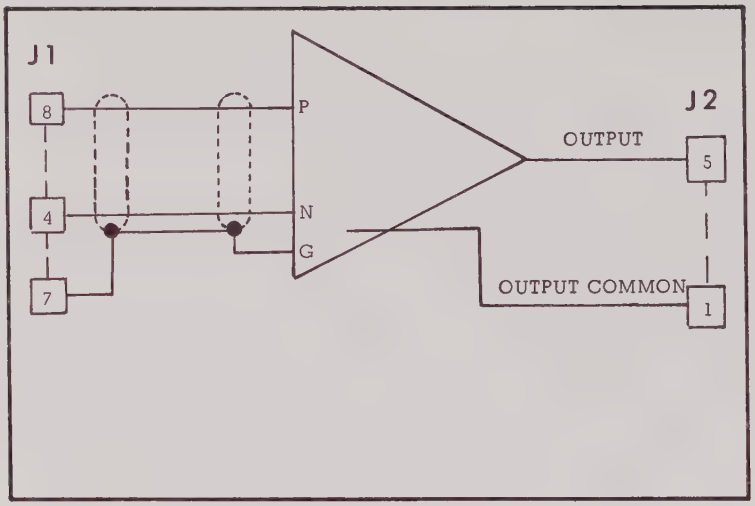
Dana Amplifiers, manufactured for domestic use, operate on 115 volts (±10 volts), 50 to 400 Hz. Units manufactured for export operate on 210 to 250 volts, 50 to 400 Hz. Power required is six watts.

NOTE

If the Amplifier has been stored for a prolonged period (5 or 6 months) without use, it is recommended that it be operated with a variable transformer, such as a Variac, at one-half line voltage for about two hours before gradually applying full power. This is done to "reform" the electrolytic capacitors in the amplifier and reduce the chance of capacitor failure.

2.3 INPUT/OUTPUT CONNECTIONS

Input and output connections to the amplifier are through eight pin connectors (J1 and J2) at the rear of the amplifier (see Figure 2.1). External connections are brought in through a mating connector. When the Dana enclosures are used, the mating connector for each amplifier is mounted on the inside back panel of the enclosure; each amplifier plugs into its corresponding connectors. When amplifiers are used singly, a single unit adapter set is normally used. The adapter set (Dana part number 402468) includes the mating connector, power cord, and clip leads for input/output signal connections.



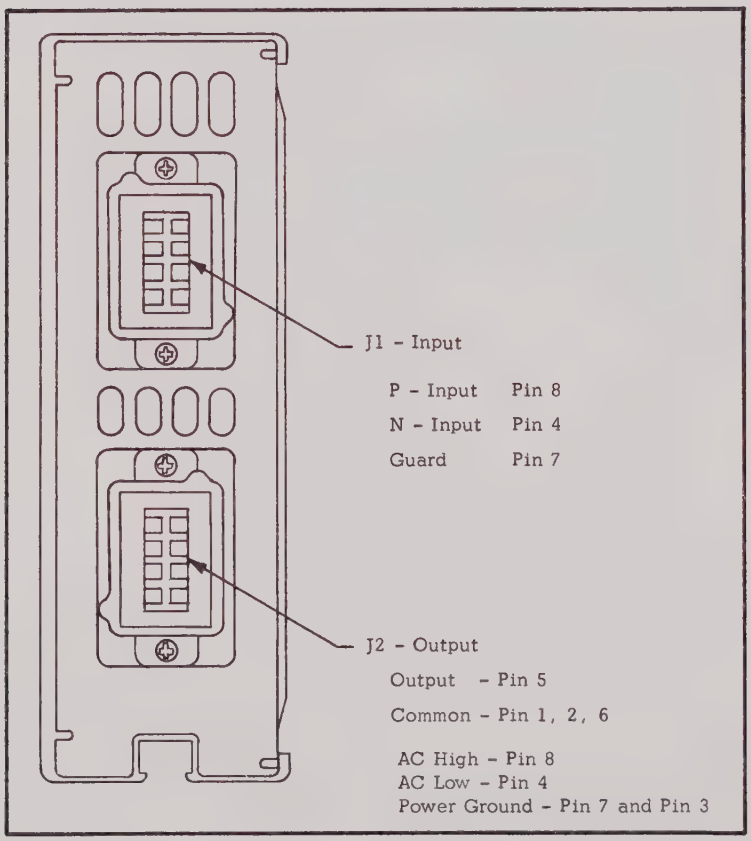

J1 - Input
P - Input Pin 8
N - Input Pin 4
Guard Pin 7
J2 - Output
Output - Pin 5
Common - Pin 1, 2, 6
AC High - Pin 8
AC Low - Pin 4
Power Ground - Pin 7 and Pin 3

Figure 2.1 - Input/Output Connections

When the 2808-1 Enclosure is used (see Figure 2.2), external connections are made directly to the solder side of the enclosure mounted connector for each amplifier. Access to connectors is gained by removing four screws holding the rear panel and allowing the top of the rear panel to drop away from the enclosure. External leads are routed through the grommet holes and soldered to the connectors.

In the 2808-2 Enclosure, conventional cable connectors are mounted on the rear panel. Connections are made by wiring to the mating connector. All pin connections are identified in Figure 2.2.

2.3.1 Power

When the Amplifier is to be operated within the 2808-1 or 2808-2 Enclosure, power is prewired and a three-wire line cord is supplied. When using the cord set, power and input/output connections are prewired. The power cord is connected to P2 of the cord set.

The ground wire of the power cord connects to the internal power supply shield of the amplifiers.

2.3.2 Input/Output Signals

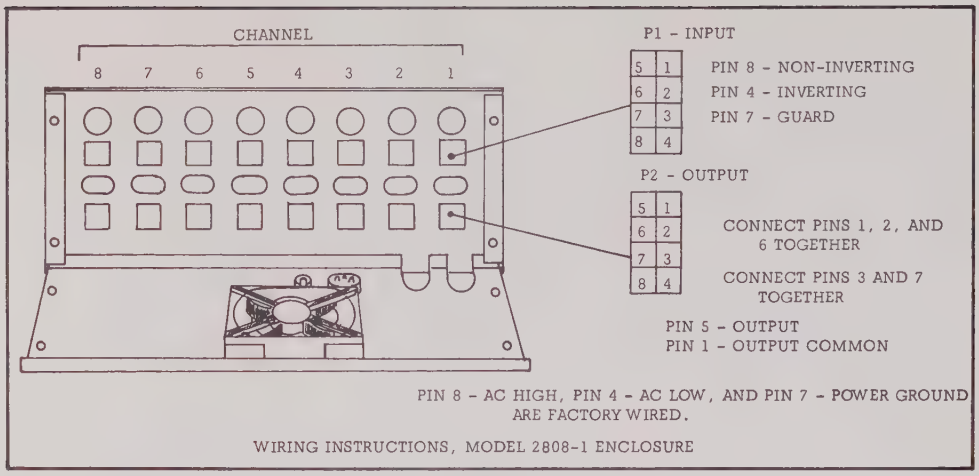
Input wiring configurations are extremely important in minimizing common mode voltages. The guard lead should be connected as close as possible to the signal source. Input and output connections are shown in Figure 2.2.

For permanent installations, low thermal solder (70% cadmium, 30% tin) should be used for all input connections to reduce thermal couple errors. For temporary or test setups, screw terminals or clips having low resistance may be used, taking suitable care to minimize thermal emf's (a few microvolts can be significant on high gain ranges).

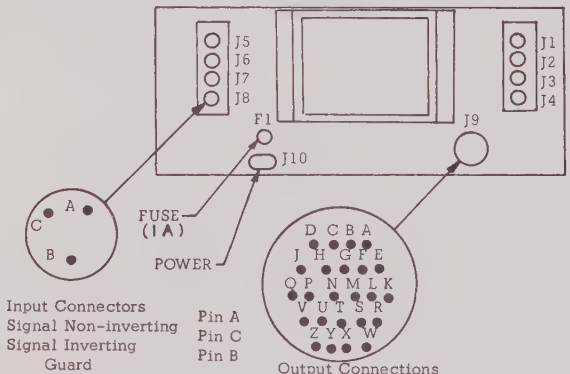
Since P and N inputs to the amplifier are symmetrical (approximately equal impedance to output common), either lead may be connected to either side of the signal source. For phasing purposes, if P is positive with respect to N, the output is positive with respect to output common.

Input leads should be two-conductor in an insulated shielded cable (Belden #8451-500, or equivalent). The shield must be soldered to the guard pin connection (pin 7 of J1 when a -1 Enclosure is used; pin B of the signal input connector for a -2 Enclosure). The unshielded portion of the leads must be kept as short as possible.

A single-conductor shielded cable is recommended for output leads. If two-conductor is used, connect one lead and shield together at either end or both ends. Solder the shield to Output Common (pin 1 of J2 for -1 enclosures; see Figure 2.2 for -2 enclosures). The enclosure chassis is connected to ground by the power cable. The lead from the output common terminal of the amplifier should be connected directly to the input common or ground of the output device.


CHANNEL
8 7 6 5 4 3 2 1
P1 - INPUT
5 1
6 2
7 3
8 4
PIN 8 - NON-INVERTING
PIN 4 - INVERTING
PIN 7 - GUARD
P2 - OUTPUT
5 1
6 2
7 3
8 4
CONNECT PINS 1, 2, AND 6 TOGETHER
CONNECT PINS 3 AND 7 TOGETHER
PIN 5 - OUTPUT
PIN 1 - OUTPUT COMMON
PIN 8 - AC HIGH, PIN 4 - AC LOW, AND PIN 7 - POWER GROUND ARE FACTORY WIRED.

WIRING INSTRUCTIONS, MODEL 2808-1 ENCLOSURE



CHANNEL	OUTPUT	OUTPUT COMMON
1	A	B
2	E	F
3	K	L
4	R	S
5	W	X
6	D	C
7	J	H
8	Q	P

CHASSIS GROUND PIN Z

NOTES: (1) Use shielded two conductor twisted pair cable for input leads. Shield is soldered to Guard Pin Connection.

(2) Single conductor shielded wire is recommended for output leads. Solder shield to output common pin.

(3) Viewing enclosure from the front, amplifiers are numbered from left to right.

	Mating Connector & Clamps	Dana Part Number
INPUT	3106 A-10 SL-3S A105-A115	601561
(8 sets required)	3057-4A-A105 w/Bush	601474
OUTPUT	3106 A-24-28P-639	601563
(1 set required)	3057-16A-639 w/Bush	601564
AC POWER	Belden Power Cord #17256	600127
(1 set required)		

Wiring Instructions, Model 2808-2 Enclosure

Figure 2.2 - Enclosure Wiring

2.4 INITIAL CHECKOUT PROCEDURES

The amplifier is accurately adjusted and carefully inspected at the factory. The following tests check basic characteristics of the amplifier to verify proper operation upon delivery. The type of damage that can be expected in shipment tends to produce gross malfunctions rather than minor changes in sensitive characteristics. More complete and precise tests and calibration procedures are included in Section 5, "Calibration".

Only three items of test equipment are required to perform initial checkout of the amplifier:

- Audio Oscillator
- Voltage Divider/Attenuator
- Oscilloscope

Standard laboratory-type instruments from any manufacturer may be used.

2.4.1 Gain Checkout

1. Connect the common or ground terminals of each item of test equipment to a single point and to the amplifier output common (pin 1 of J2). Connect this point to ground. Make all measurements relative to this point (see Figure 2.3).

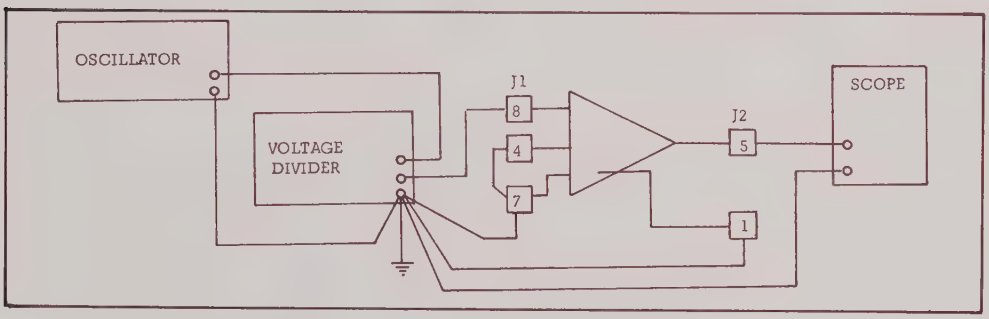


Figure 2.3 - Gain Test Setup

2. Set voltage divider to minimum output — zero, if possible.

3. Apply power to amplifier. Observe amplifier output on oscilloscope. It should be within a few millivolts of ground and change only very slightly as the amplifier GAIN switch is rotated.

4. Set the VERNIER gain adjustment fully counterclockwise.

5. Set the GAIN selector switch at the highest gain position. If the amplifier is equipped with a Gain Multiplier switch (V2), set it to 1.0.

6. Remove scope lead from amplifier output and connect scope to the oscillator output. Adjust oscillator for 20 volts, peak-to-peak, at 100 Hz.

7. Set voltage divider to the reciprocal of the maximum gain setting, 1/K. (For example, at maximum gain of 1000, set divider to 0.001.)

8. Return the scope to the amplifier output, pin 5 of J2. The scope should now indicate approximately the same value, 20 volts peak-to-peak, observed at the oscillator output. (The term "approximately" is used because of the limited capability of an oscilloscope to compare two magnitudes accurately.)

9. Verify that there is no obvious noise or other unexplained distortions on the oscilloscope trace.

2.4.2 Frequency Response Checkout

1. Use test setup exactly as connected for Gain checkout. Set amplifier GAIN control at maximum; vernier adjustment to minimum. Connect scope to oscillator output; set oscillator frequency to 20 kHz. (Gains 20 to 1000; 10kHz for gains below 20 or above 1000).

2. Set oscillator output at 20 volts, peak-to-peak (on scope).

3. Remove scope lead from oscillator and connect to amplifier output pin 5 of J2. Adjust voltage divider for amplifier output amplitude equal to that observed in step 2.

4. Compare voltage divider setting with zero — or minimum output position. The difference should be no less than 3dB, or approximately 30%.

2.4.3 Common Mode Rejection

1. Short the amplifier input leads and the input guard lead (pins 8, 4, and 7 of J1). Connect all three to oscillator output.

2. Connect oscilloscope to amplifier output (pin 5 of J2).

3. Set oscillator output to 20 volts, peak-to-peak, at 60 Hz.

4. Set amplifier GAIN switch to 1000.

5. Observe amplifier output on scope. The output due to common mode is normally not detectable above the wideband noise of the amplifier. Common mode rejection can be calculated as follows:

$$CMR = \frac{20 \text{ Volts (P-P)} \times K}{\text{Output Voltage (P-P)}}$$

Common mode rejection may be measured more closely by following the procedures of paragraph 5.3.1, Section 5.

SECTION 3

OPERATION

3.1 MODES OF OPERATION

The Dana Amplifier can be used in any of the four operating modes illustrated below.

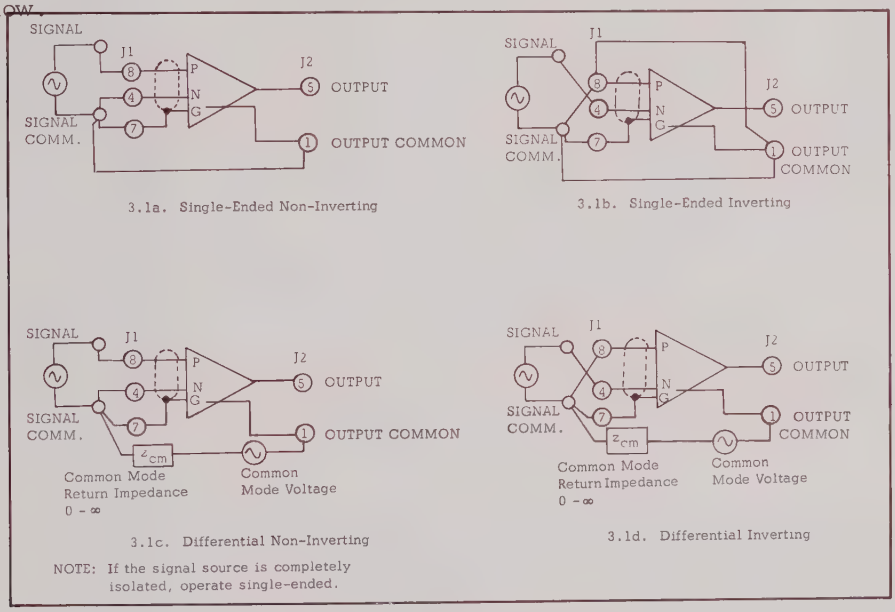


Figure 3.1 - Modes of Operation

3.2 CONTROLS

3.2.1 Gain Selector Switch

The GAIN switch is rotated to select the desired gain of the amplifier. The gains which can be selected vary with the options specified. Gain positions are tabulated below.

Options	Gain Switch Positions
V1 & V2	20, 50, 100, 200, 500, and 1000
V3	100, 200, 500, 1000, 2000, and 5000

3.2.2 Multiplier Switch (Option V2)

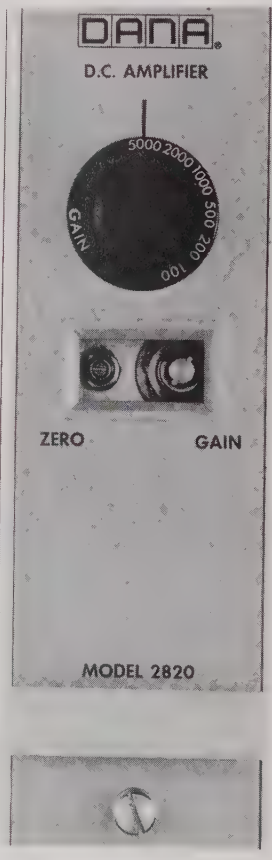
The Multiplier switch is mounted concentrically with the GAIN selector switch. It has two positions, X.01 and X1. In X.01 position, it reduces the gain selected by a factor of 100. For example, effective gains would be 0.2, 0.5, 1, 2, 5 and 10. In the X1 position, amplifier gain is exactly as inscribed on the switch.

3.3 OPERATIONAL ADJUSTMENTS

3.3.1 ZERO Adjustment

ZERO is a screwdriver adjustment on the front panel of the amplifier. It is used to set the output voltage to zero volts with no input. It is adjusted in the following manner:

1. Apply power to the amplifier and any adjoining heat-producing equipment and allow amplifier to stabilize (approximately 30 minutes),
2. Set GAIN selector switch to lowest gain position.
3. Return the input P(J1-8) and N(J1-4) leads to output common (j2-1).
4. Connect voltmeter or scope to amplifier output (J2-5) and common (J2-1).
5. Adjust ZERO for zero amplifier output. Counterclockwise rotation corrects for a positive output; clockwise rotation corrects for a negative output.



Model 2820-V3

3.3.2 GAIN Adjustment

This is a screwdriver adjustment which serves as a vernier adjustment of gain selected by the GAIN selector switch. The adjustment varies each gain position by a factor of 2.5:1 — providing continuous gain selection throughout all available ranges.

3.4 OPERATING PROCEDURES

After installation of the amplifier as described in Section 2, operation consists simply of selecting the appropriate gain. The amplifier is ready for use immediately with zero stabilility achieved within 30 minutes.

SECTION 4

CIRCUIT DESCRIPTION

4.1 INTRODUCTION

This section contains an electrical description of each circuit in the amplifier. A block diagram of the Model 2820 is shown in Figure 4.1.

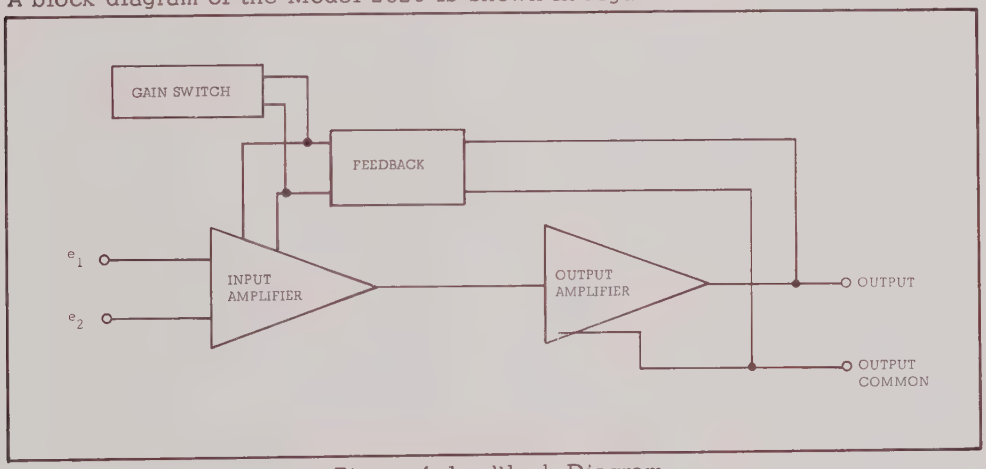


Figure 4.1 - Block Diagram

The forward loop consists of the Input Amplifier and the Output Amplifier. The loop is closed by the feedback network. The Input Amplifier amplifies the potential difference between the two inputs. When one input goes positive and the other input goes negative with respect to common, the output of the amplifier is proportional to the difference of the amplitudes. These signals are referred to as "normal mode signal" (also referred to as "difference" or differential signals). The potentials common to both inputs are referred to as "common mode signals" and are rejected by the amplifier. The normal mode signals and the common mode signals are defined below.

Normal Mode Signal $= e_1 - e_2$

Output (E_O) $= (e_1 - e_2)$ (Gain)

Common Mode Signal $= \dfrac{e_1 + e_2}{2}$

In single ended operation, a signal is applied to one input while the other input is common; therefore, the output is proportional to the amplitude of the one signal applied.

Figure 4.2 shows the amplifier responding to normal mode signals and rejecting the common mode signal (one-half) of the bridge supply voltage. In practical applications, there would be additional common mode potentials due to stray fields and other causes. These potentials represented by "e_x" are also rejected.

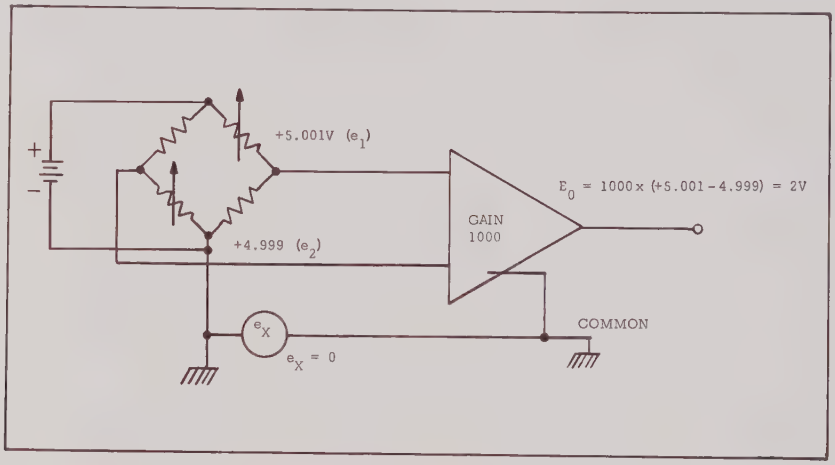


Figure 4.2 - Normal Mode and Common Mode Response

4.2 NORMAL MODE AMPLIFIER

Figure 4.3 shows a potentiometric amplifier. This type of amplifier is a potentiometric device, since the feedback achieves a high effective input impedance by the same principle as the common "null balance" approach to precision measurements. In both cases, the effective input impedance approaches infinity at null. In the potentiometric amplifier, impedance is limited by factors such as leakage and practical values of loop gain.

Examining the feedback system, it can be seen that the feedback is of proper phase to cancel the effect of the input signal; nowever, the cancellation leaves a small "error" signal of sufficient magnitude to support the 5-volt output. In the example, if the open loop gain (gain without feedback) of the circuit were 140 dB, the approximate residual error signal would be $5V/10^7$ or 0.5uV (e_e in the figure).

To achieve the desired gain stability and linearity, the open loop gain is considerably greater than the closed loop gain. By keeping this ratio sufficiently high, the "closed loop" or "net gain" is essentially determined by the feedback elements alone.

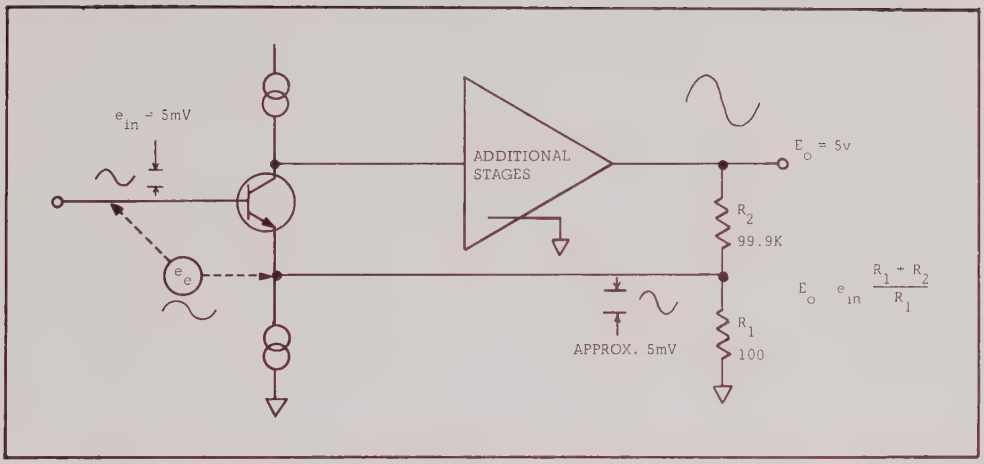


Figure 4.3 - Simplified Potentiometric Amplifier (Gain of 1000)

Figure 4.4 shows two potentiometric amplifiers connected in a differential configuration. One-half of the normal mode voltage ($e_{NM}/2$) appears at e_1 while the other one-half of the normal mode voltage appears at e_2. As in Figure 4.3, a 5 millivolt signal at each of e_1 and e_2 will be 5 volts output at each potentiometric amplifier. With the differential amplifier stage as shown in Figure 4.5, the outputs of the balanced differential stages are combined in the summing amplifier which transfers one directly and inverts the other. This is in keeping with the normal mode signal characteristics of $e_1 - e_2$. Signals of common polarity or phase will cancel at the summing stage, the degree of cancellation dependent on their relative magnitudes.

Input lines (e_1, e_2) are connected to the bases of a pair of matched silicon transistors (dual transistors in a single case) and circuit parameters are adjusted to obtain equal characteristics in each stage. A unique aspect of the circuit is the technique employed in controlling these parameters for stable operation over wide temperature ranges.

4.3 COMMON MODE AMPLIFIER

Although the Normal Mode Amplifier provides a degree of common mode rejection (CMR = 60 to 70 dB with balanced source), it is insufficient for high accuracy data systems. The primary deficiency of the circuit is the low impedance between the input lines and common - too low to materially reduce common mode currents. This deficiency is overcome by the use of a separate Common Mode Amplifier (CMA) which senses the common mode voltage at the input and forces the emitters of the "input pair" of the normal mode amplifier to the same potential (neglecting bias). This "bucking" voltage allows very little current to flow from either input to output common, increasing the intrinsic impedance to common.

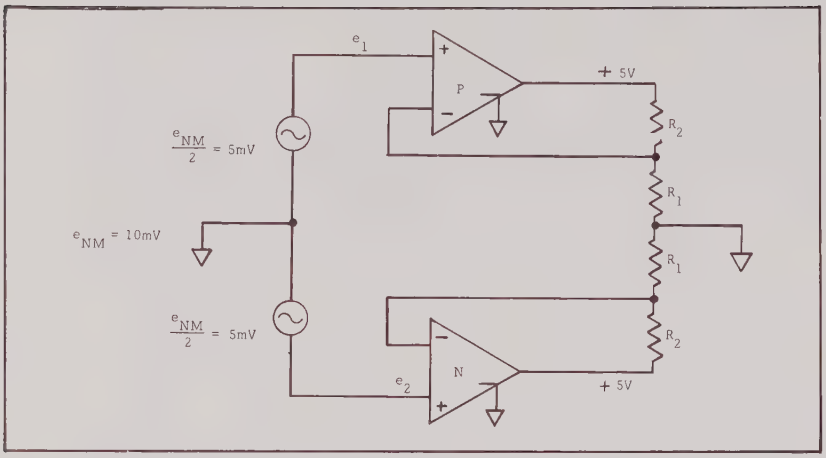


Figure 4.4 - Potentiometric Amplifiers in Differential Configuration

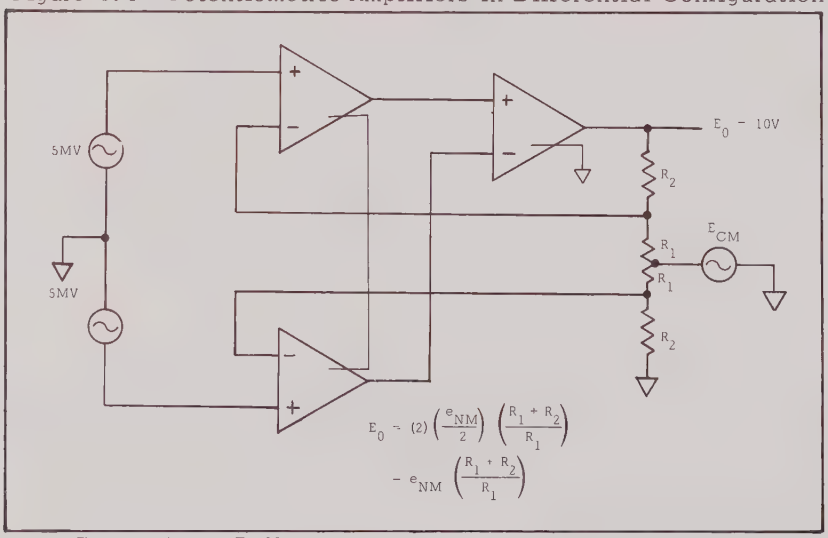


Figure 4.5 - Differential Stage for Summation of Inputs

Figure 4.6 shows the relationship of the normal mode amplifier and the common mode amplifier. The output of the common mode amplifier (E_{CM}) is connected to the junction of the R_1 resistors.

The voltages, e_1 and e_2, appear at the voltage divider as shown in Figure 4.6. The "bucking" voltage is supplied by the common mode amplifier.

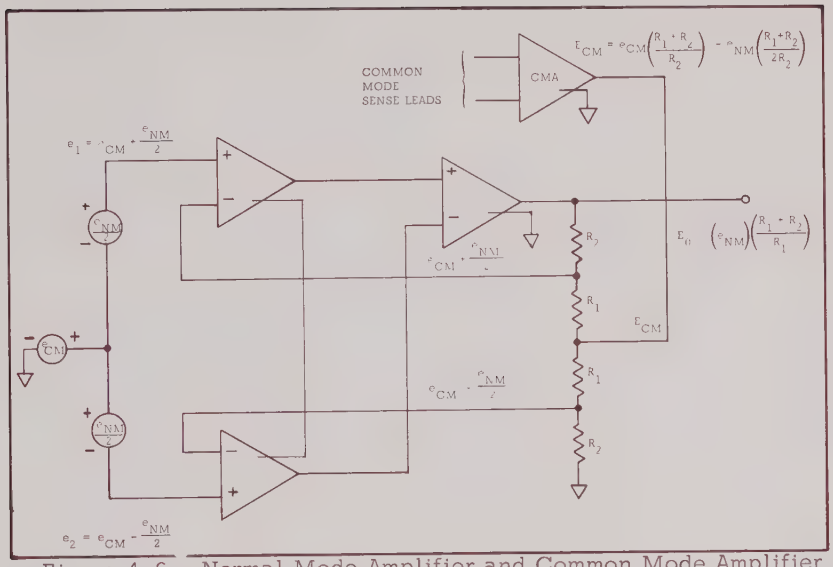


Figure 4.6 - Normal Mode Amplifier and Common Mode Amplifier

Consider the upper-half of the voltage divider and the lower-half of the voltage divider as shown in Figure 4.7. The upper-half of the voltage divider is bounded by the two voltages E_O and E_{CM}. The voltage at E_{01} is equal to

$$E_{01} = E_O - \left(E_O - E_{CM}\right)\left(\frac{R_2}{R_2 + R_1}\right)$$

and is the "bucking" voltage to effectively cancel $e_{CM} + \frac{e_{NM}}{2}$.

The lower-half of the voltage divider is bounded by E_{CM} and common. The voltage at E_{02} is equal to

$$E_{02} = E_{CM}\left(\frac{R_2}{R_1 + R_2}\right)$$

and is the "bucking" voltage to effectively cancel

$$e_{CM} - \frac{e_{NM}}{2} .$$

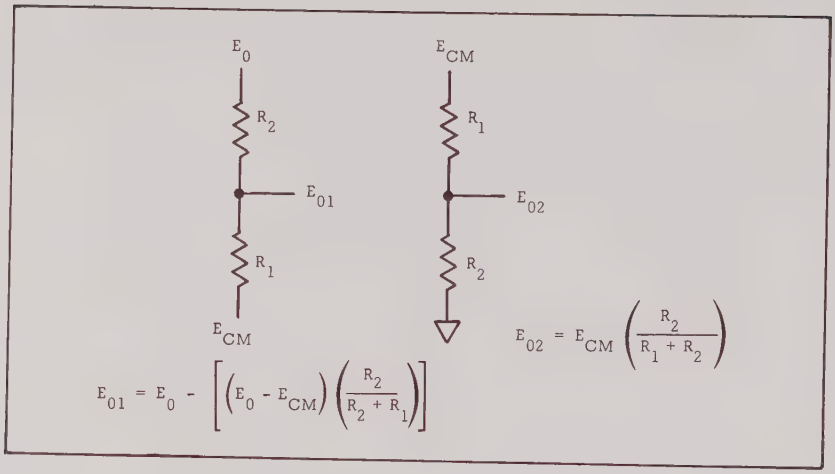


Figure 4.7 - Voltage Dividers

The common mode voltage (E_{CM}) from the common mode amplifier required to satisfy the equations is

$$E_{CM} = e_{CM}\left(\frac{R_1 + R_2}{R_2}\right) - e_{NM}\left(\frac{R_1 + R_2}{2R_2}\right)$$

The gain of the normal mode amplifier is set by inserting a resistor R_X as shown in Figure 4.8. Resistor R_X does not influence the value of E_{CM} and may be varied without interfering with the common mode compensation.

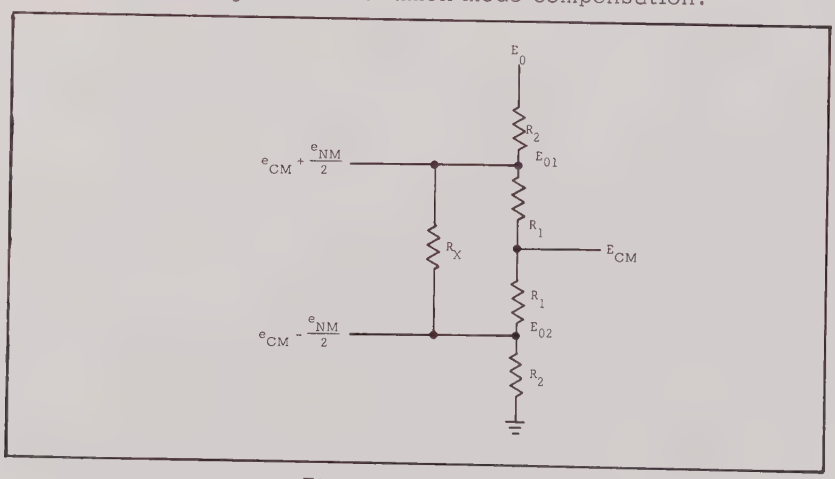


Figure 4.8 - Gain Set

4.4 INPUT AMPLIFIER

The Input Amplifier can now be shown as in Figure 4.9a. Differential input signals cause out-of-phase signals to be developed across the input pair's respective collector resistors. Under these conditions, the drop across the collector summing resistor (R36 in Figure 4.9a) remains constant; however, a voltage source common to both input lines (e_{CM}) causes in-phase collector current variations which add through R36 and produce a signal proportional to the common mode potential, providing an input to the CMA. As illustrated in Figure 4.9a, the CMA couples a feedback signal to the emitters of the input pair through R42 and R44. This signal is of the proper phase to cancel the effect of the input potential and maintain the sum of the two collector currents constant. Cancellation is complete except for a small residual error voltage necessary to maintain the output of the CMA very near the common mode potential (ignoring feedback insertion loss).

For convenience, the Common Mode Amplifier has been described as if it were a single-ended device referenced to ground. However, the CMA is a differential amplifier much like the Normal Mode Amplifier and, as such, responds to the difference between its input terminals. In the actual circuit, one of the CMA input terminals is connected to the lower side of the input stage collector summing resistor and the other to a passive divider connected between the input pair emitters and the top of the collector summing resistor (Figure 4.9a).

If this circuit is closely examined, it can be seen that the various circuit elements form a simple bridge. This identity is established in Figure 4.9b. In operation, the application of a common potential to the input transistors tends to unbalance the bridge by changing the conductance of the input pair. This effect is opposed by driving the lower end of the bridge (or the emitters of the input pair) with the output of the CMA. This feedback effectively cancels the change in conductance and restores the bridge to balance.

As previously stated, the parameters of the input stage are carefully adjusted for nearly identical characteristics. Once established, they cannot be allowed to change when the circuit is subjected to common mode potentials. From Figure 4.9 it can be seen that the entire input circuit is floating between two constant current generators. Since it has been established that the active elements in the bridge circuit (transistors) are continuously balanced against passive elements (R36, R39, R50, R41), it becomes apparent that the constant current sources will also serve to maintain constant voltage conditions across the bridge (constant I x constant R = constant E). This means that, as the lower part of the bridge is driven up and down synchronously with the common mode potentials, the voltage at the top of the bridge varies with the same relative magnitude. This "bootstrapping" effect raises the intrinsic common mode rejection of the input pair to the high values required for high accuracy systems.

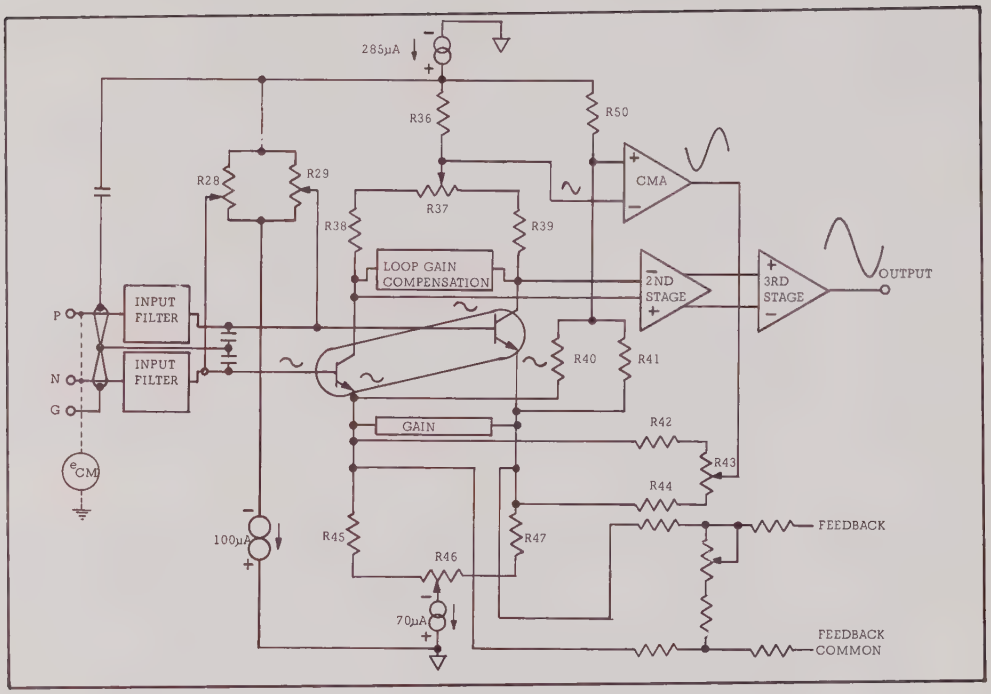


Figure 4.9a - Input Amplifier

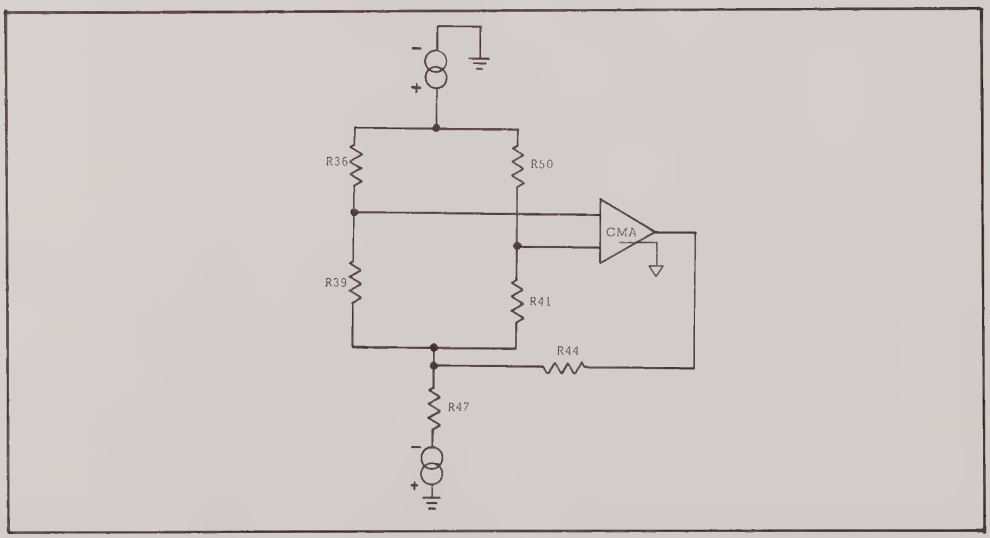


Figure 4.9b - Equivalent Bridge

Potentiometers R28 and R29 are the N-input and P-input offset-current zero adjustments to minimize the current flow-through the input terminals.

The gain and loop-gain compensation blocks shown in Figure 4.9 are networks selected from the front panel GAIN select switch.

4.5 OUTPUT AMPLIFIER

The Output Amplifier (Figure 4.10) consists of a voltage-to-current converter stage followed by a single ended operational amplifier. The single ended amplifier is a complementary symmetry class AB power amplifier with negative feedback.

A separate power supply provides a positive voltage and a negative voltage capable of delivering up to 100 milliamperes to the load. The power supply is shown as batteries in Figure 4.11.

The current supplies are controlled by common emitter drivers and are driven with respect to common in accordance with the input signal. Transistor Q20 controls the positive current through the load. As the positive current increases through the load, the output voltage at the common connection node of the current supplies goes negative. As the negative current increases through the load (controlled by transistor Q22), the output voltage goes positive.

The negative current limit is determined by adjusting R91 (10 ohm potentiometer), the positive current limit is determined by adjusting R92 (10 ohm potentiometer). The current adjustment for each potentiometer is approximately 95-150 milliamperes. Diode clamps, CR17 and CR18, will conduct when the voltage across either the emitter resistor of the output driver (Q20) or the emitter resistor of the current limiter (Q21) reaches +0.6 volt. Diode clamps, CR19 and CR20, will conduct when the voltage across either the emitter resistor of the output driver (Q22) or the emitter resistor of the current limiter (Q23) reaches -0.6 volt.

The short-circuit current limit of the Output Amplifier is approximately 150 milliamperes. The current limit for a 100 ohm load is approximately 120 milliamperes.

Transistor Q17 (see schematic drawing of Output Amplifier in Section 7) is a constant current bias generator (one milliampere).

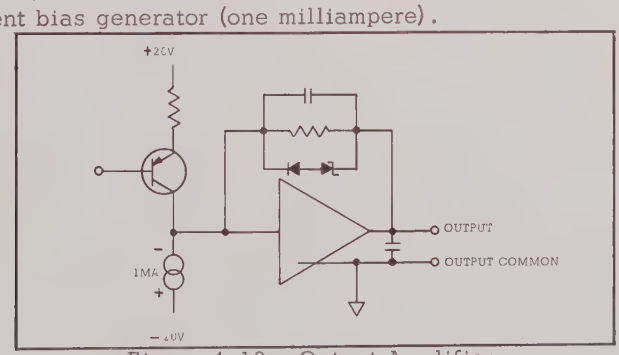


Figure 4.10 - Output Amplifier

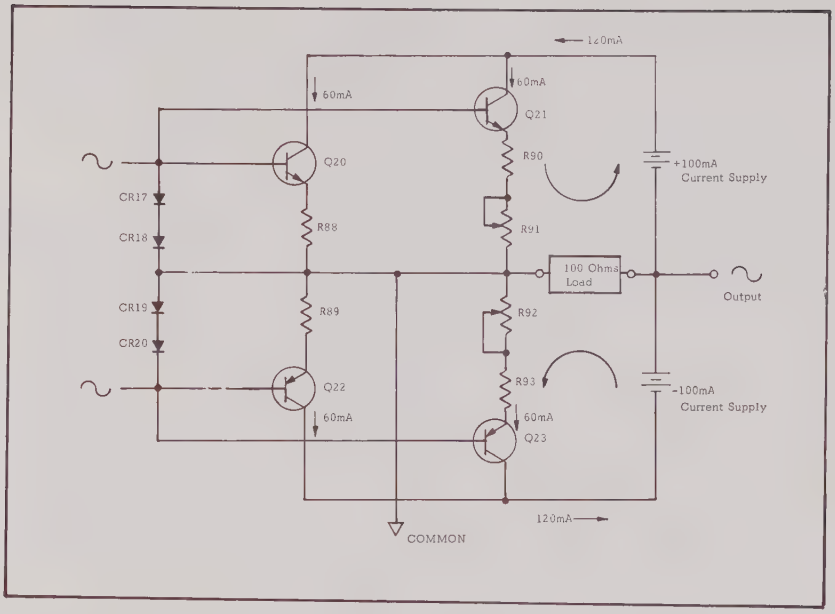


Figure 4.11 - Output Drivers and Current Limiters

4.6 FEEDBACK CIRCUIT

The differential input of the amplifier requires a feedback network slightly more complex than the simple divider that was shown in Figure 4.3. To illustrate, consider the case where one input is connected to a positive signal and the other to a negative signal. It would appear that the proper bipolar feedback for both inputs could not be derived from a single output terminal; however, this is not the case.

Figure 4.12 shows the equivalent feedback network of the amplifier. For the purpose of the initial discussion, assume no connection between points A and B, and that the amplifier has somehow arrived at the proper ten-volt output for a ten-millivolt input (gain of 1000). It can be seen that the voltage difference between the two feedback lines is the required 10 millivolts; however, both lines are approximately +5 volts above common. This is obviously intolerable and the circuit will not function until a connection is made between points A and B. It should be emphasized that the +5 volts is common to both input transistors and would tend to unbalance the common mode bridge just as an external common mode potential would do. The only difference in the two situations is the fact that the "feedback" common mode voltage is internally generated and tends to drive the input emitters in lieu of the bases. The latter results in one less phase inversion for internally generated common mode signals, producing an output from the CMA fo the opposite output which goes negative until the feedback lines become approximately +5 millivolts and -5 millivolts with respect to common.

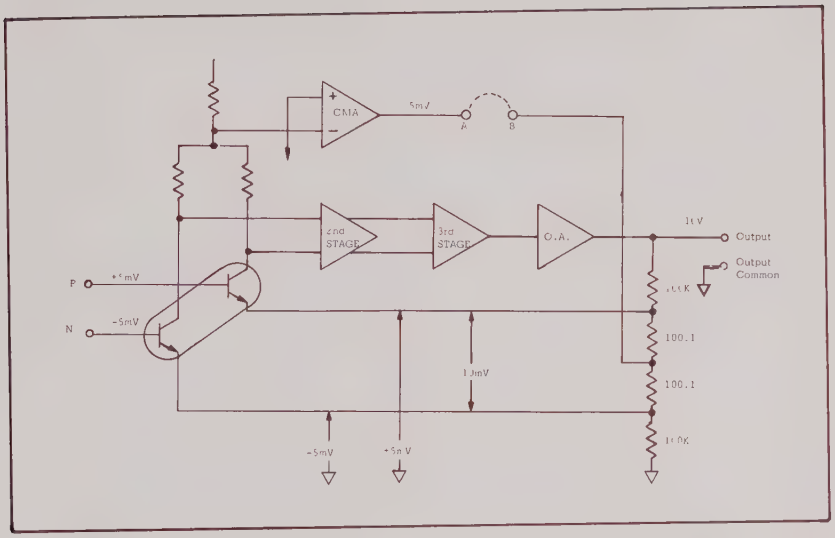


Figure 4.12 - Equivalent Feedback Network for Gain of 1000

It can now be seen that the CMA will not tolerate the bridge to be unbalanced at any time, whether the common mode potential is introduced internally or externally. More specifically, the collector currents are never permitted to shift in the same direction but can only vary by equal and opposite amounts in response to differential input signals. This fact holds true regardless of the symmetry of the input signals. For example, consider the situation where one input is tied to common and the other is driven with a 10 millivolt AC signal. The CMA assumes the proper signal level so that equal and opposite error signals exist between the base and emitter of each input transistor. The final quiescent conditions are shown in Figure 4.13.

4.7 ADDITIONAL CIRCUIT DETAILS

For ease of explanation, several circuit details were intentionally overlooked. Specifically, the diagrams used to illustrate certain fundamental points inferred a quiescent voltage level of zero at several points that are normally several volts positive or negative with respect to ground. Circuit operation as described is fundamentally accurate except that signal levels are relative to the initial conditions. The static bias condition of the input pair is of particular interest since it is related to input current uncertainty. These stages are initially forward biased and, though the base idling currents are quite low, they would develop an offset voltage if allowed to flow through the external signal source resistance.

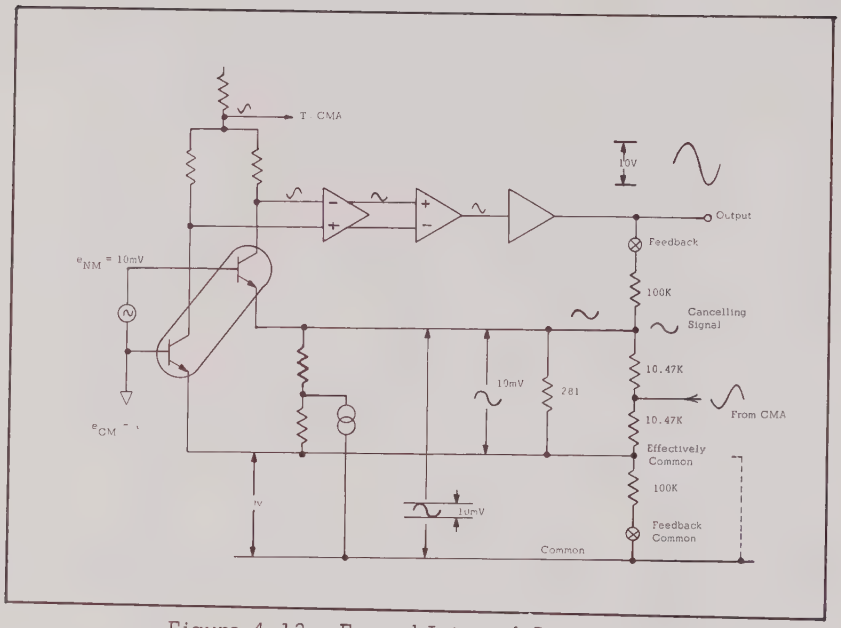


Figure 4.13 - Forced Internal Symmetry

To minimize this effect, each input line is connected to a source that shunts this current to the amplifier's internal supplies. An adjustment is provided for each input line, permitting the input current to be periodically rezeroed in the field (R28, R29 in Figure 4.9). To prevent common mode loading, these sources are floated between a constant current generator and the top of the common mode bridge. Since both input leads and the collector supply move together with the common mode potential, the current through the base resistors remains very nearly constant. This infers that the impedance to common potentials is a large magnification of the apparent 5 megohms in each base lead (on the order of 1000 megohms); and also points out that the quiescent base current is virtually undisturbed by common mode potentials.

Another important point is the relationship between the magnitude of the common mode potential and the voltage level at the output of the CMA. If the source of common mode is external, the output of the CMA is 10% greater than the applied voltage; if the source is internal (one-half of the output signal), the output of the CMA is $-E_{out}/20$. This relationship is solely determined by the ratio of the respective feedback resistors.

SECTION 5

CALIBRATION

5.1 RECOMMENDED TEST EQUIPMENT

- OSCILLOSCOPE: X-Y inputs; bandpass, DC-500 kHz; calibrated deflection factors of one millivolt to 20 volts per centimeter accurate within 3%; input impedance, one megohm paralleled by less than 50 picofarad.

- OSCILLATOR: Frequency range, 5 Hz - 500 kHz; accuracy, ±2%; frequency response, ±1 dB; adjustable output voltage, 160 milliwatts (10 volts) into 600 ohms rated load, 20 volts open circuit.

- VACUUM TUBE VOLTMETER: Voltage range, 0.1 millivolt to 300 volts; dB range, -72 to +52 dB; frequency range, 10 Hz to 1 MHz accurate within ±2% (50 Hz - 500 kHz); input impedance, 10 megohms paralleled by less than 50 picofarad.

- ATTENUATOR: Attenuation to 120 dB in 1dB steps; DC to 1 MHz accurate within ±1 dB; power capacity, 5 watts.

- DC MILLIVOLTMETER (optional)

- Dana Model 2095 Test Panel (optional) or Adapter Set 2801 (P/N402468).

The Dana Model 2095 Amplifier Test Panel provides a convenient means of testing and calibrating Dana amplifiers. The panel requires that only the amplifier input, output, and power be connected to the panel with no further reconnections required. All input and output configurations necessary to calibrate or test the amplifier are set up by switches and controls mounted on the panel. The panel is shown in Figure 5.1.

5.2 LISSAJOUS FIGURES FOR COMMON MODE ADJUSTMENTS

The output null of the amplifier is checked with the Lissajous figures as shown in Figure 5.2. The adjustments for the quadrature error and amplitude error are mentioned in paragraph 5.3.1. Figure 5.2a shows the amplifier output at null for maximum common mode rejection.

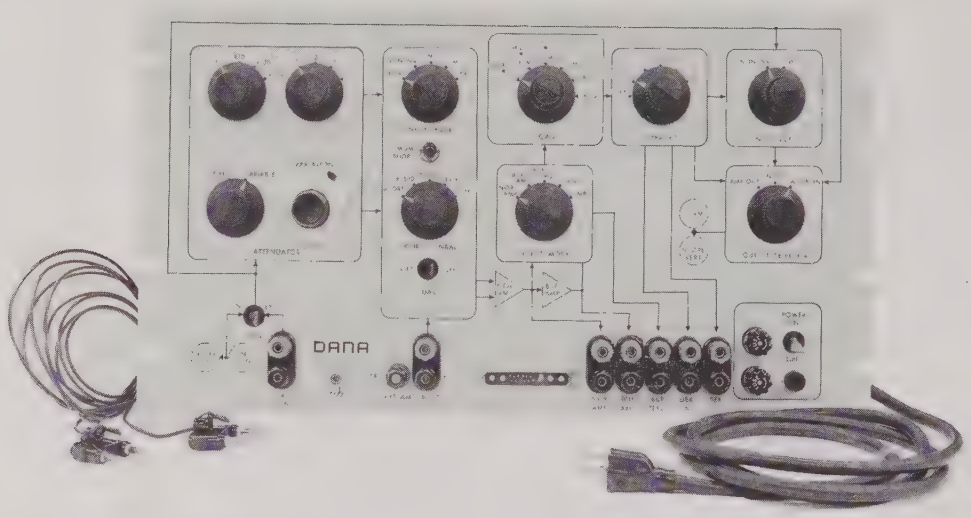


Figure 5.1 - Model 2095 Amplifier Test Panel

The V1 and V3 gain options quadrature error and amplitude error are adjusted by adjusting the following components:

Capacitor C15 - quadrature error
Potentiometer R43 - amplitude error

The V2 option has the above adjustments when the Multiplier switch is in the X1 position. Another set of adjustments calibrates the quadrature and amplitude error for the X.01 Multiplier switch position. These adjustments are:

Capacitor C5 - quadrature error
Potentiometer R10 - amplitude error

The procedures for the above adjustments are detailed in paragraph 5.3.4.

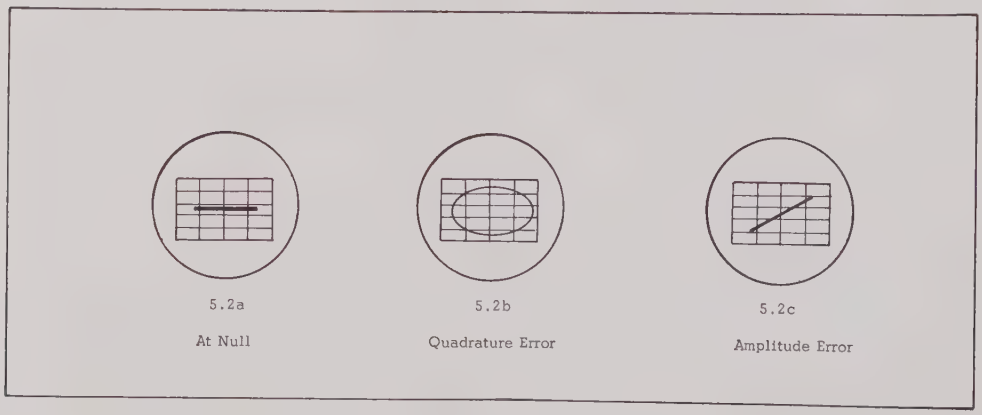


Figure 5.2 - Lissajous Figures

5.3 CALIBRATION PROCEDURES

In addition to the following calibration procedures, certain performance characteristics should be checked periodically and internal adjustments made as required. These measurements are described in section 5.4. The procedure below should be performed in the order listed.

All adjustments are easily accessible through the side of the amplifier. Physical location of the adjustable components is shown in Figure 5.3.

> CAUTION
>
> Common mode potentials appear between the guard box and chassis; therefore, an insulated screwdriver or adjustment tool (J.F.D Adjustment Tool 5284) should be used to make the calibration adjustments of the input amplifier.

5.3.1 Common Mode Adjustments

The amplifier has two controls that affect common mode rejection by adjusting the symmetry of the input circuit. R43 compensates for resistive unbalance and C15 adjusts the capacitive symmetry. Physical location of the two components is shown in Figure 5.3.

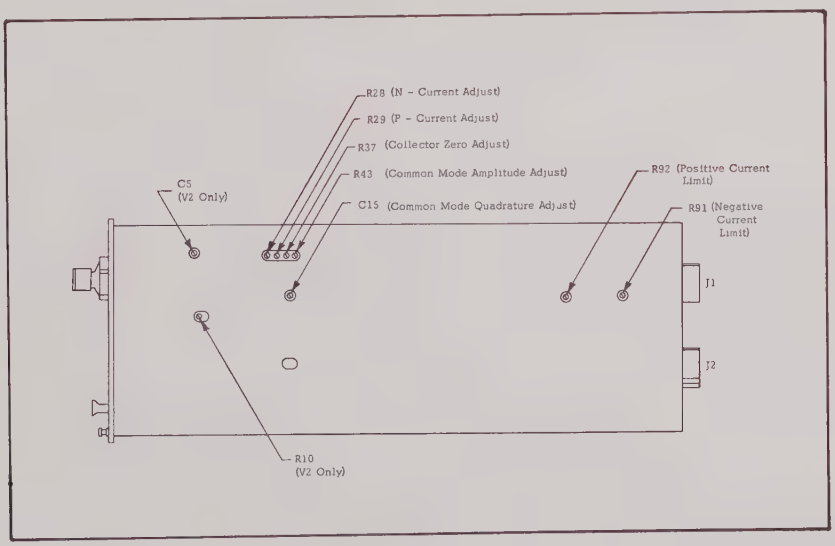


Figure 5.3 - Amplifier Adjustments, Physical Location

Adjustment procedures are as follows:

1. Connect inputs P(J1-8), N(J1-4), and guard (J1-7) to the high side of a signal generator, returning the low side to output common (J2-1).

2. Connect the signal generator to the X-axis of an oscilloscope with the X-axis sensitivity set to 5 volts/cm.

3. Connect amplifier output (J2-5) to the Y-axis of the oscilloscope through a single pole, low pass filter consisting of a 16K resistor and a 0.01 microfarad capacitor.

4. If the amplifier is equipped with a V2 option, place the multiplier switch to the X1 position.

5. Set the oscillator to 20 volts (P-P) at 60 Hz and amplifier GAIN to 1000.

6. Adjust R43 and C15 for minimum deflection as shown in Figure 5.2a.

5.3.2 COLLECTOR ZERO ADJUSTMENT

In addition to the operational ZERO adjustment on the front panel, the amplifier is equipped with an internal zero adjustment (R37). Procedure for making the adjustment is as follows:

1. Connect amplifier inputs P(J1-8), N(J1-4), and guard (J1-7) to output common (J2-1).

2. Connect an oscilloscope or millivoltmeter to output (J2-5) and common (J2-1).

3. Set amplifier GAIN switch to lowest gain position (20 for V1, V2 options; 100 for V3 option); adjust the front panel ZERO adjustment (R46) for minimum reading on the millivoltmeter. Record any residual offset.

4. Set amplifier GAIN switch to highest gain position (1000 for V1, V2 options; 5000 for V3 option); adjust the internal collector ZERO adjustment (R37) for the same offset recorded in step 4.

5. Repeat steps 3 and 4 until the output remains the same on both the highest and lowest gain positions.

5.3.3 Input Current Adjustment

This adjustment minimizes current flow through the input terminals. For most accurate adjustment, the following procedures should be performed after the Collector Zero adjustment.

1. Set amplifier GAIN switch to the gain of 1000. (V1, V2 options; set to 5000 for V3 option).

2. Connect input terminals P(J1-8), N(J1-4), and guard (J1-7) to output common (J2-1).

3. Connect oscilloscope to output (J2-5) and common (J2-1). Set vertical deflection to 5mV/cm. Record amplitude of offset voltage at output.

4. Disconnect N(J1-4) terminal from output common; insert 1k resistor in series and reconnect to output common (J2-1).

5. Adjust R28, the N current control, for same offset recorded in step 3.

6. Remove 1k resistor from N(J1-4) lead and reconnect N(J1-4) lead to output common (J2-1) and guard (J1-7). Remove P(J1-8) lead, insert 1k resistor in series, and reconnect to output common (J2-1) and guard (J1-7).

7. Adjust R29, the P current control, for same offset recorded in step 3.

8. Repeat steps 4 through 7 (because of interaction of R28 and R29) until P(J1-8) and N(J1-4) offset voltages are equal. Remove the resistor; connect P and N to output common (J2-1) and guard (J1-7). Repeat the original offset measurement as made in step 3. All three voltages should be equal. If the original offset voltage has changed, repeat the entire procedure.

5.3.4 Input Gain Symmetry Adjustment

Option V2 is equipped with a gain multiplier switch. A potentiometer (R10) and a capacitor (C5) establish gain symmetry between the two input lines when the gain multiplier switch is in the X.01 position. This adjustment permits common mode rejection to be optimized when operating from balanced sources. R10 and C5 are adjusted as follows:

1. Set amplifier GAIN to 1000 and the input multiplier switch to X.01.

2. Connect the N(J1-4) and P(J1-8) input terminals to the high side of a signal generator set to 60 Hz and maximum output (not to exceed 60 volts, peak). Return the low side of the signal generator to output common (J2-1).

3. Connect an oscilloscope to amplifier output terminals (J2-5) and (J2-1) and adjust R10 and C5 for minimum deflection.

5.3.5 Output Zero Adjustment

This adjustment sets the zero of the Output Amplifier by means of the ZERO adjustment on the front panel.

1. Connect input terminals N(J1-4) and P(J1-8) to output common (J2-1). Connect this point to ground.

2. Connect an oscilloscope across the output (J2-5) and common (J2-1).

3. Vary the ZERO adjustment (on front panel) for minimum reading on oscilloscope. Note this voltage for further reference. (This voltage represents residual offset).

5.4 TESTS OF AMPLIFIER CHARACTERISTICS

The following measurements check basic amplifier operating characteristics — such as gain, bandpass, etc.

5.4.1 DC Gain Measurement

1. Connect test setup as shown in Figure 5.4. (The signal source need not be particularly accurate or stable, but the voltage divider must be extremely accurate. The null detector must be isolated and resolve less than 1mV).

2. Set DC voltage source at 10 volts.

3. Adjust voltage divider so that there is no change in null detector indication when the input polarity is reversed by the reversing switch. Note ratio of voltage divider setting. Calculate gain as follows:

$$K = \frac{1}{h}$$

where K = amplifier gain
h = ratio of voltage output to input of divider.

5.4.2 Linearity Measurement

Ideally, gain should be independent of the magnitude of the output voltage from minus full scale to plus full scale. Since the Dana Amplifier's departure from this ideal is small, the null balance method of the gain measurement is again used. Linearity can be measured immediately after the DC gain measurement (see Figure 5.4). The test setup shall remain the same except that a variable DC voltage is required.

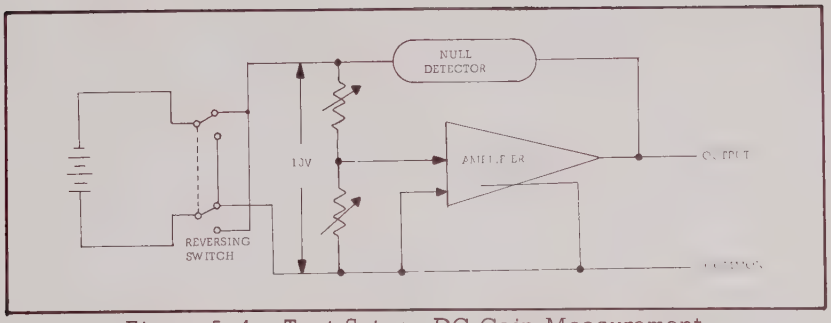


Figure 5.4 - Test Setup, DC Gain Measurement

Steps 1 and 2 are followed as for DC Gain Measurement (5.4.1). The input voltage is then varied from minus full scale to plus full scale, and the peak reading of the null detector recorded. The linearity in percentage can be calculated as follows:

$$\frac{\text{Peak Null Detector Reading (Volts) X 100}}{\text{Full Scale (10 Volts)}}$$

5.4.3 AC Gain Measurement

The technique used for DC gain measurement can be extended to AC if the phase lag in the amplifier is compensated and a suitable null detector is used. If these types of measurements are anticipated, a special transformer and phase correction network may be procured from Dana; however, in general, a simpler and more direct method is described below:

1. Connect test setup as shown in Figure 5.5. (The divider should be of sufficiently low impedance to prevent errors due to source resistance. The output meter should be a good quality AC voltmeter having a mirrored scale and at least 100 minor divisions.
2. Place the monitor switch to position 1 and set the signal generator to an output of approximately 7 volts RMS at 60 Hz.
3. Select a minor division on the meter's best scale (maximum resolution and legibility) and adjust the output of the signal generator very carefully to place the needle of the meter directly on this marker. Use the mirror to avoid parallax.
4. Set the monitor switch to position 2 and adjust the voltage divider for exactly the same reading established in step 2.
5. Carefully observing the meter, move the monitor switch alternately between positions 1 and 2 to ensure that the reading is exactly the same in both positions.
6. Compute the gain of the amplifier by taking the reciprocal of the ratio set up on the voltage divider.

5.4.4 Bandwidth Measurement

Bandwidth is measured by determining the difference in AC gain at low and at high frequencies. Since there is seldom a need to define bandwidth with extreme accuracy, the measurement procedures may be shortened as follows:

1. Use same test setup as for AC Gain Measurement, Figure 5.5.

2. Follow steps (1) through (4) of AC Gain Measurement with the signal generator set to 60 Hz.

3. Increase the frequency to 20kHz (gains 20-1000; 10kHz for gains less than 20 and greater than 1000) and record the difference in readings between switch positions 1 and 2. If the meter has 100 minor divisions, each division represents approximately 1.4% of full scale.

In making the above measurement, it must be remembered that the bandwidth specifications apply for source impedances up to 350 ohms. When checking bandwidth make certain this value is not exceeded. If a low impedance divider is not available, it may be necessary to improvise one.

5.4.5 High Frequency Linearity

Linearity is determined by the following equation:

$$\text{Linearity (in \%)} = 100\frac{E_{out} - KE_{in}}{E_{out}\ \text{(full scale)}}$$

To measure high frequency linearity, an extremely accurate AC/AC ratiometer is recommended such as the Dana Model 5400/060 or 5740. The measurement procedures are listed below:

1. Connect test setup as shown in Figure 5.6. Set the signal generator 7 volts RMS at 60 Hz. Set amplifier GAIN to 1000.

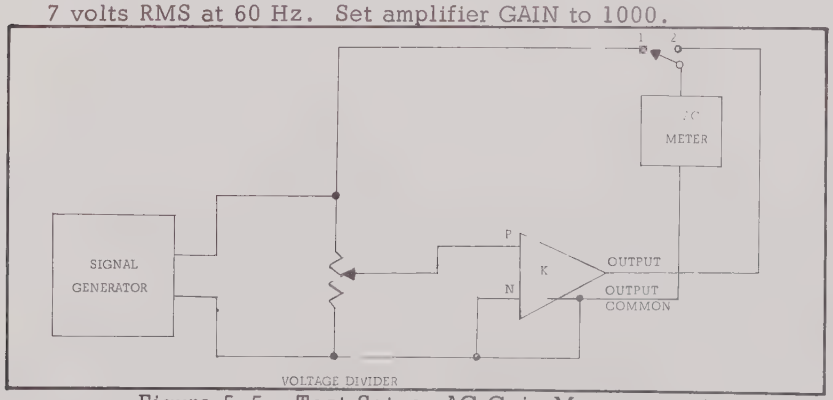


Figure 5.5 - Test Setup, AC Gain Measurement

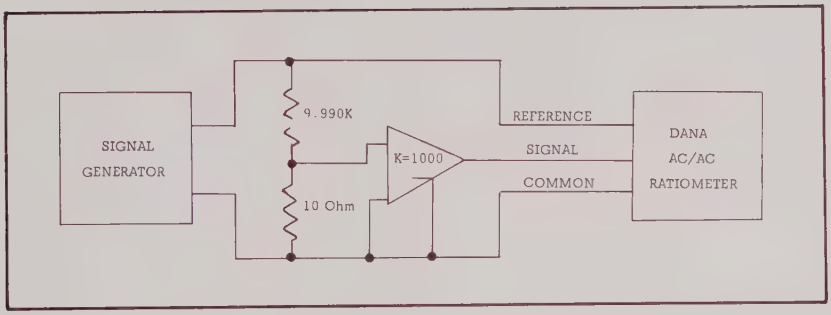


Figure 5.6 - Test Setup, High Frequency Linearity

2. Trim the input divider and/or the amplifier vernier control until the absolute ratio is 0.99990 (displayed on ratiometer as 9.9990). This reading indicates a slight gain error; however, this is not important to the linearity measurement and allows the latter to be made with greater resolution.

3. Leaving all other adjustments set, increase the signal generator frequency to 2 kHz and observe the new reading on the ratiometer.

4. Compute linearity as follows:

$$\text{Linearity in \%} = \frac{\text{Reading 1 - Reading 2}}{1000}$$

If no range changes are involved, the result can be more quickly computed by allowing 0.001% for each digit of difference.

SECTION 6

TROUBLESHOOTING

6.1 GENERAL

Conventional instrumentation amplifiers are often difficult to troubleshoot, since the average malfunctions cause abnormal readings or signal levels to appear throughout the loop. By comparison, the Dana Amplifier is far easier to service since the various direct-coupled circuits can be readily isolated and inspected independently.

6.2 DANA REPAIR AND SERVICE POLICY

Details of Dana's repair and service policy may be found in the Dana Warranty at the rear of the manual. Items for repair should include a copy of the Dana return form describing the reason for return. Units not accompanied by this information must be held without action pending receipt of this information. A copy of this Repair/Return form is included at the rear of this manual. Additional copies may be obtained from Dana Laboratories or from Dana Sales representatives.

6.3 TROUBLESHOOTING GUIDES

Component failures may cause bias points to shift and loop gain to change such that the output voltage will move from near zero volts to a large positive or negative d-c voltage level. These levels are greater than ± 12 volts and are called "positive lockup" and "negative lockup". Three malfunctions in the amplifier can cause output lockup. These are:

- Open or short circuit
- Defective component
- Drastic change in component characteristics

The troubleshooting guides help to isolate sections of the amplifier where the malfunction may exist. The sections can be isolated without having to break or disconnect any of the loops in the amplifier.

The step-by-step troubleshooting procedure verifies that there are no open or shorted components and that the current generators are supplying the proper currents to the circuits.

A preliminary check is to be made prior to using the troubleshooting guides. Short the P input (J1-8), N input (J1-4), and Guard (J1-7) together and connect these leads to output common (J2-1). The output voltage (J2-5) with respect to common should be near zero (zero $\pm$250 millivolt). If the output voltage is near zero, proceed to the calibration section of this manual. If the output voltage is greater than plus or minus 12 volts, the output is at lockup. Apply the troubleshooting guides in the following sequence:

1. Power Supply
2. Output Amplifier
3. Normal Mode Amplifier
4. Common Mode Amplifier
5. Feedback Network

> CAUTION
>
> The guides assume that the troubleshooter is experienced in troubleshooting solid state circuits. Non-standard practices can cause more damage to the amplifier.

Reference is made to the schematic number and assembly number where the circuit designators are located. These numbers appear at the bottom of the troubleshooting guide.

Unless the troubleshooting guide indicates otherwise, the output voltage is monitored at J2-5 (output) and J2-1 (output common).

6.4 TROUBLESHOOTNG EQUIPMENT

All of the transistors in the amplifier can be checked in the circuit. The only exception is the output transistor Q15 of the Common Mode Amplifier (see schematic 430603). Diode CR12 is across the collector to emitter leads of transistor Q15.

The following equipments are needed to troubleshoot the amplifier:

- A Simpson VOM (volt-ohmmeter) Model 260 or equivalent, can be used to check the forward and reverse resistances of the semiconductors. Disconnect the AC power prior to making these measurements.
- A 2000 ohms, 1/4 watt, carbon resistor.

- An oscilloscope or a voltmeter capable of measuring positive and negative voltages without manually changing the polarity for monitoring the output voltage of the amplifier.

- A precision ohmmeter.
  The tolerance value of most precision resistors in the amplifier is 0.1%.

- Dana Cord Set - Part Number 402469.

6.5 COMPONENT REPLACEMENT

Defective components should be replaced with components identical to the original component. Precision wirewound resistors with 0.1% tolerances should be replaced with wirewound resistors of the same tolerance value. The characteristics of the components are critical for temperature stability, zero stability, and gain stability.

The first stage dual (Q2) and the second stage dual (Q5) of the normal mode amplifier should be ordered from the factory. The first stage dual transistor is part of a kit along with four precision resistors. This stage should be replaced as a unit. The Dana part number for the first stage kit is 400708. The kit consists of a selected dual transistor (Q2) and selected wirewound resistors R38, R39, R45, and R47.

The Dana part number for the second stage dual (Q5) of the normal mode amplifier is 201285.

Dana recommends that the components be ordered from the Dana service department. Specify the part and Dana part number for the defective component.

The amplifier should be recalibrated after replacing components. Refer to the calibration procedures in Section 5.

6.6 AMPLIFIER DISASSEMBLY

Remove eight, number 6, Phillips flat-head screws from the aluminum support (right-hand side of the amplifier as viewed from the front panel).

To remove the cover, place the amplifier in the left hand and pull the cover toward the rear of the amplifier as shown in Figure 6.1a.

To remove the aluminum support, remove six, number 4, Phillips pan-head screws holding the circuit board assembly to the aluminum support. Three screws are at the top of the circuit board assembly; the other three screws are at the bottom of the circuit board assembly. Place the amplifier in the left hand and push the circuit board assembly as shown in Figure 6.1b.

The guard box encloses the Input Amplifier and Feedback Network. To remove the guard box cover, remove two, number 4, Phillips pan-head screws at the top of the cover and lift the cover from the guard box. The guard box is shown in Figure 6.1c.

The etched-circuit side of the Input Amplifier is electrically guarded by a fiber-glass guard plate. The guard plate is held to two standoffs by two, number 4, Phillips flat-head screws. Remove the guard plate to probe the etched circuit side of the Input Amplifier.

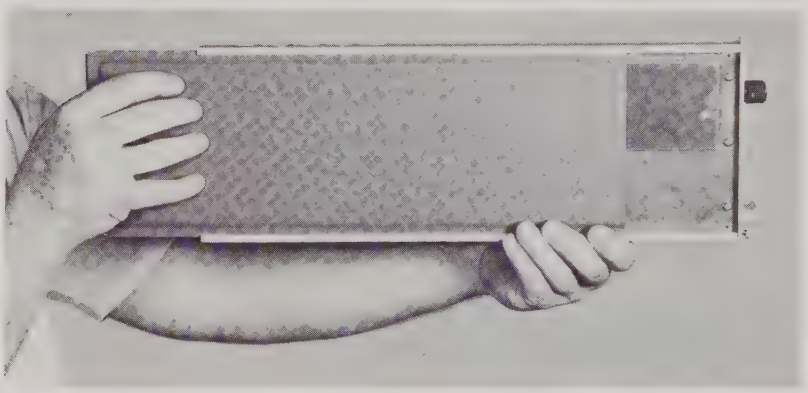


Figure 6.1 a

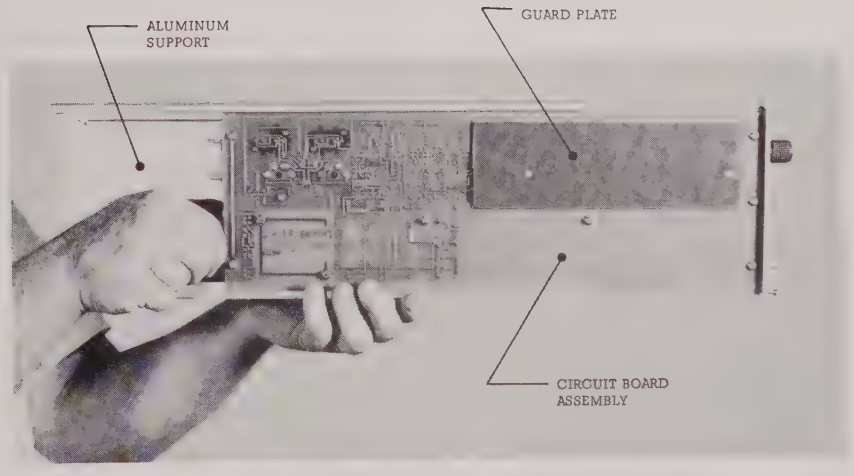


Figure 6.1 b

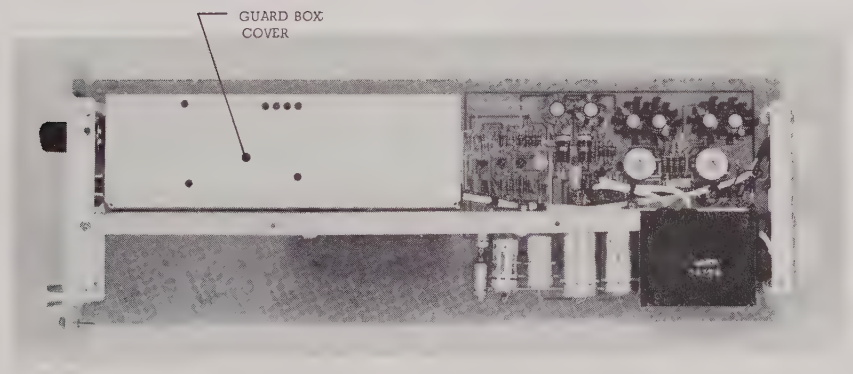
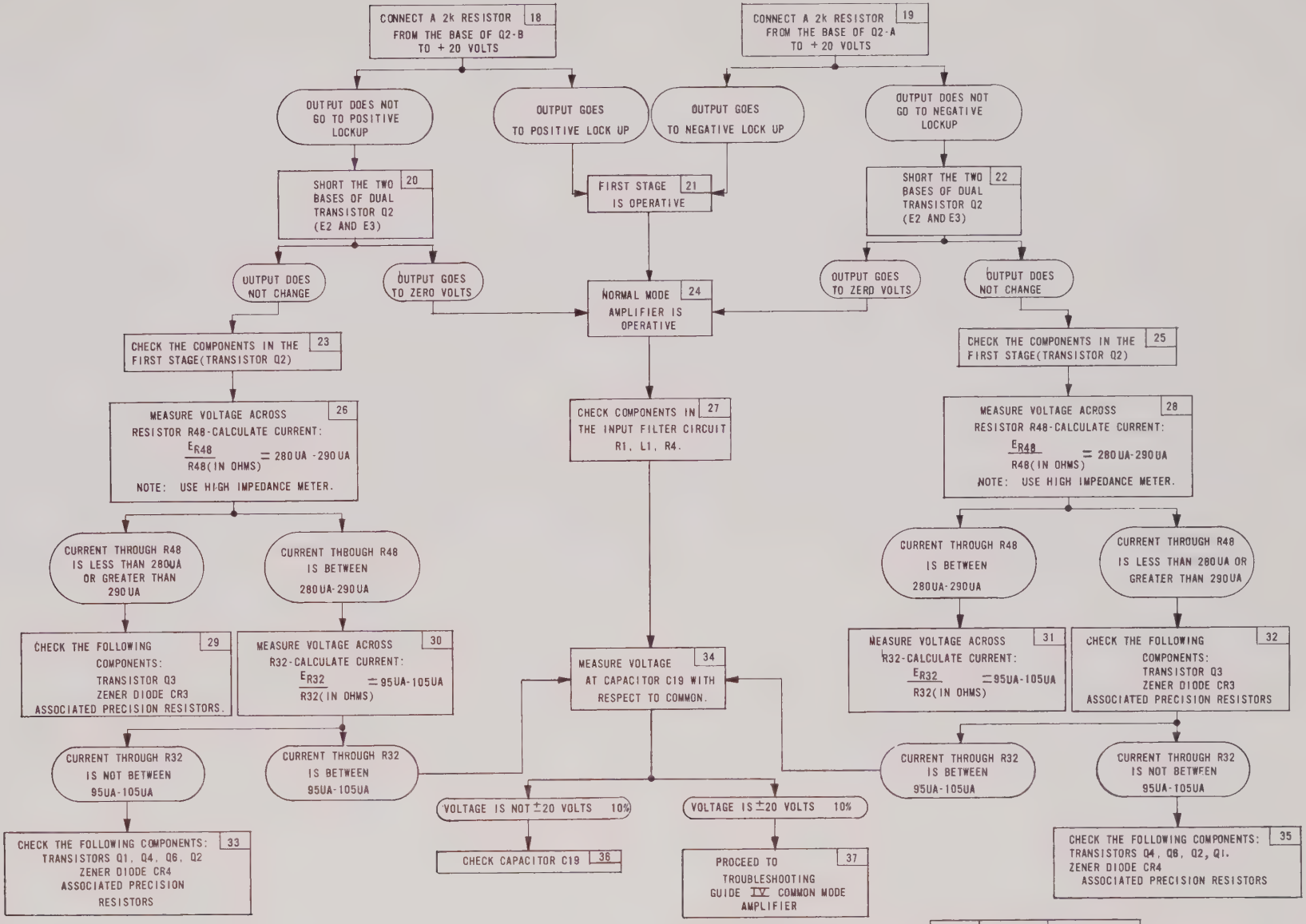


Figure 6.1 c

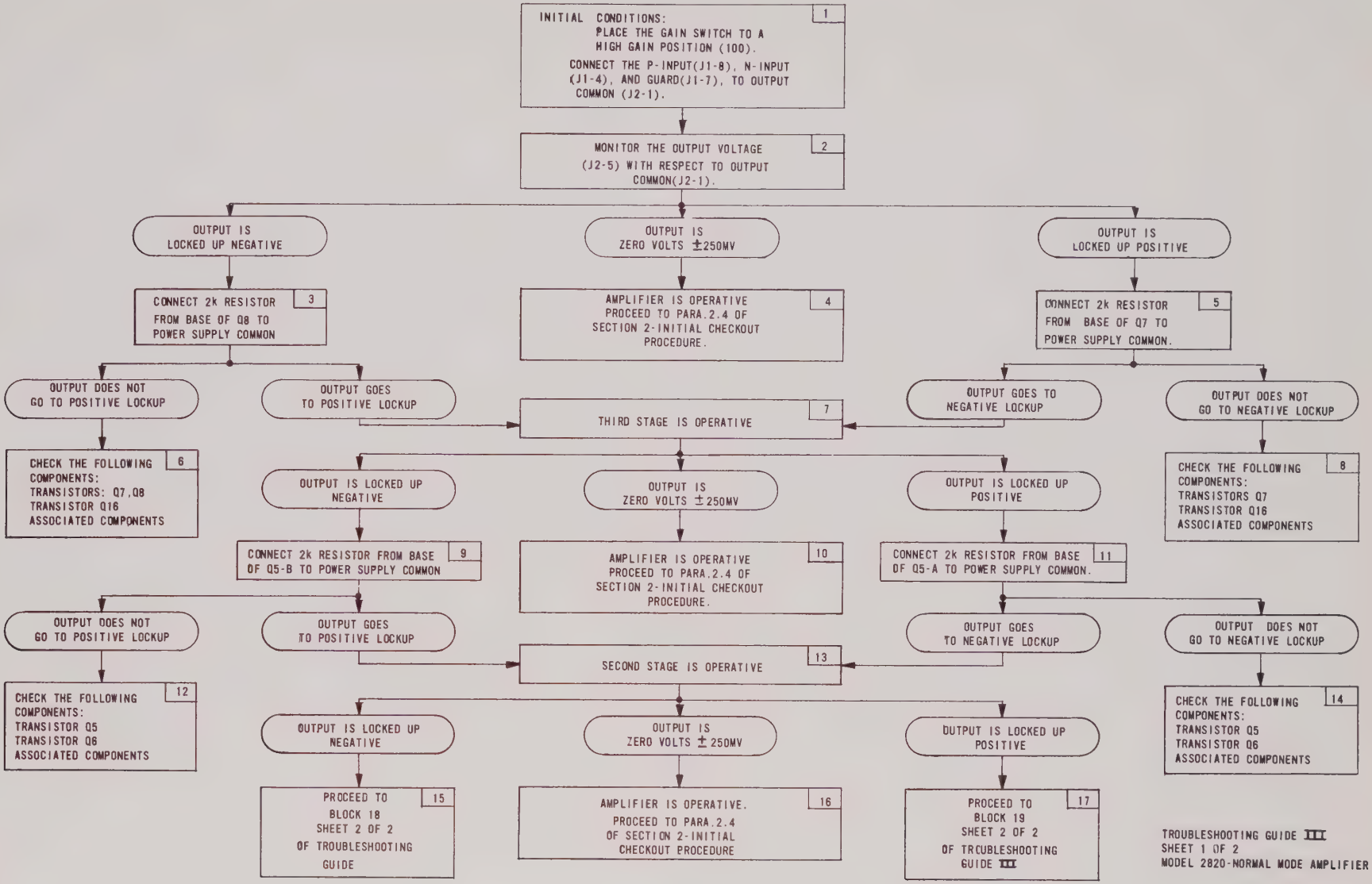
TROUBLESHOOTING GUIDES

Power Supply I
Output Amplifier II
Normal Mode Amplifier (2 sheets) III
Common Mode Amplifier IV
Feedback Network V

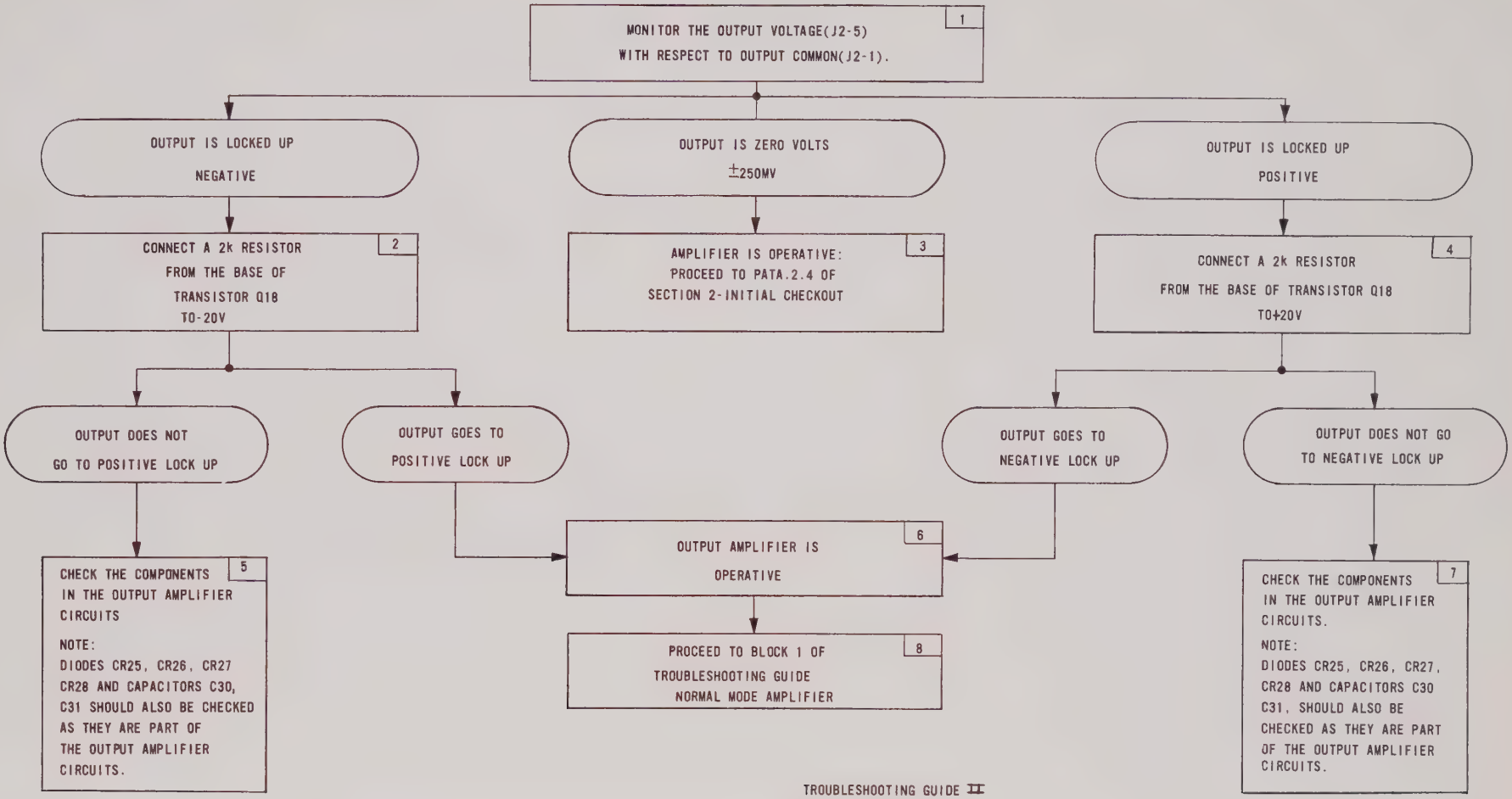

CONNECT A 2k RESISTOR FROM THE BASE OF Q2-B TO +20 VOLTS 18
CONNECT A 2k RESISTOR FROM THE BASE OF Q2-A TO +20 VOLTS 19
OUTPUT DOES NOT GO TO POSITIVE LOCKUP
OUTPUT GOES TO POSITIVE LOCK UP
OUTPUT GOES TO NEGATIVE LOCK UP
OUTPUT DOES NOT GO TO NEGATIVE LOCKUP
SHORT THE TWO BASES OF DUAL TRANSISTOR Q2 (E2 AND E3) 20
FIRST STAGE IS OPERATIVE 21
SHORT THE TWO BASES OF DUAL TRANSISTOR Q2 (E2 AND E3) 22
OUTPUT DOES NOT CHANGE
OUTPUT GOES TO ZERO VOLTS
OUTPUT GOES TO ZERO VOLTS
OUTPUT DOES NOT CHANGE
NORMAL MODE AMPLIFIER IS OPERATIVE 24
CHECK THE COMPONENTS IN THE FIRST STAGE(TRANSISTOR Q2) 23
CHECK THE COMPONENTS IN THE FIRST STAGE(TRANSISTOR Q2) 25
MEASURE VOLTAGE ACROSS RESISTOR R48-CALCULATE CURRENT: E R48 / R48(IN OHMS) = 280UA -290UA NOTE: USE HIGH IMPEDANCE METER. 26
CHECK COMPONENTS IN THE INPUT FILTER CIRCUIT R1, L1, R4. 27
MEASURE VOLTAGE ACROSS RESISTOR R48-CALCULATE CURRENT: E R48 / R48(IN OHMS) = 280UA-290UA NOTE: USE HIGH IMPEDANCE METER. 28
CURRENT THROUGH R48 IS LESS THAN 280UA OR GREATER THAN 290UA
CURRENT THROUGH R48 IS BETWEEN 280UA-290UA
CURRENT THROUGH R48 IS BETWEEN 280UA-290UA
CURRENT THROUGH R48 IS LESS THAN 280UA OR GREATER THAN 290UA
CHECK THE FOLLOWING COMPONENTS: TRANSISTOR Q3 ZENER DIODE CR3 ASSOCIATED PRECISION RESISTORS. 29
MEASURE VOLTAGE ACROSS R32-CALCULATE CURRENT: E R32 / R32(IN OHMS) = 95UA-105UA 30
MEASURE VOLTAGE AT CAPACITOR C19 WITH RESPECT TO COMMON. 34
MEASURE VOLTAGE ACROSS R32-CALCULATE CURRENT: E R32 / R32(IN OHMS) = 95UA-105UA 31
CHECK THE FOLLOWING COMPONENTS: TRANSISTOR Q3 ZENER DIODE CR3 ASSOCIATED PRECISION RESISTORS 32
CURRENT THROUGH R32 IS NOT BETWEEN 95UA-105UA
CURRENT THROUGH R32 IS BETWEEN 95UA-105UA
CURRENT THROUGH R32 IS BETWEEN 95UA-105UA
CURRENT THROUGH R32 IS NOT BETWEEN 95UA-105UA
VOLTAGE IS NOT ±20 VOLTS 10%
VOLTAGE IS ±20 VOLTS 10%
CHECK THE FOLLOWING COMPONENTS: TRANSISTORS Q1, Q4, Q6, Q2 ZENER DIODE CR4 ASSOCIATED PRECISION RESISTORS 33
CHECK CAPACITOR C19 36
PROCEED TO TROUBLESHOOTING GUIDE IV COMMON MODE AMPLIFIER 37
CHECK THE FOLLOWING COMPONENTS: TRANSISTORS Q4, Q6, Q2, Q1. ZENER DIODE CR4 ASSOCIATED PRECISION RESISTORS 35

TROUBLESHOOTING GUIDE III
SHEET 2 OF 2
MODEL 2820 -NORMAL MODE AMPLIFIER

OPTION	SCHEMATIC	ASSEMBLY
V1	430603	402303, 402305
V2	430604	402304, 402305
V3	430602	402390, 402305

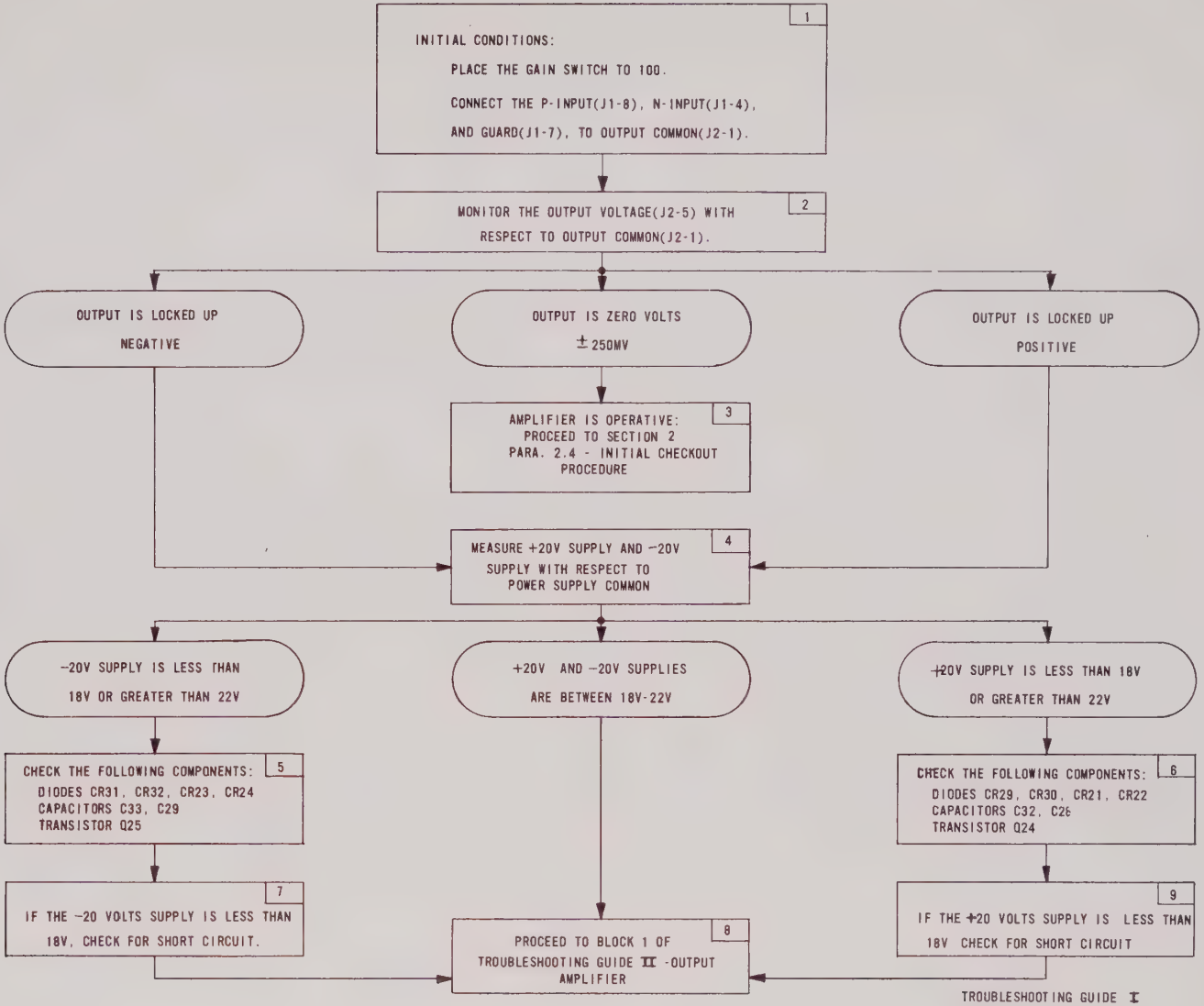

1
INITIAL CONDITIONS:
PLACE THE GAIN SWITCH TO A HIGH GAIN POSITION (100).
CONNECT THE P-INPUT(J1-8), N-INPUT (J1-4), AND GUARD(J1-7), TO OUTPUT COMMON (J2-1).
2
MONITOR THE OUTPUT VOLTAGE (J2-5) WITH RESPECT TO OUTPUT COMMON(J2-1).
OUTPUT IS LOCKED UP NEGATIVE
OUTPUT IS ZERO VOLTS ±250MV
OUTPUT IS LOCKED UP POSITIVE
3
CONNECT 2k RESISTOR FROM BASE OF Q8 TO POWER SUPPLY COMMON
4
AMPLIFIER IS OPERATIVE PROCEED TO PARA.2.4 OF SECTION 2-INITIAL CHECKOUT PROCEDURE.
5
CONNECT 2k RESISTOR FROM BASE OF Q7 TO POWER SUPPLY COMMON.
OUTPUT DOES NOT GO TO POSITIVE LOCKUP
OUTPUT GOES TO POSITIVE LOCKUP
OUTPUT GOES TO NEGATIVE LOCKUP
OUTPUT DOES NOT GO TO NEGATIVE LOCKUP
7
THIRD STAGE IS OPERATIVE
6
CHECK THE FOLLOWING COMPONENTS:
TRANSISTORS: Q7,Q8
TRANSISTOR Q16
ASSOCIATED COMPONENTS
OUTPUT IS LOCKED UP NEGATIVE
OUTPUT IS ZERO VOLTS ±250MV
OUTPUT IS LOCKED UP POSITIVE
8
CHECK THE FOLLOWING COMPONENTS:
TRANSISTORS Q7
TRANSISTOR Q16
ASSOCIATED COMPONENTS
9
CONNECT 2k RESISTOR FROM BASE OF Q5-B TO POWER SUPPLY COMMON
10
AMPLIFIER IS OPERATIVE PROCEED TO PARA.2.4 OF SECTION 2-INITIAL CHECKOUT PROCEDURE.
11
CONNECT 2k RESISTOR FROM BASE OF Q5-A TO POWER SUPPLY COMMON.
OUTPUT DOES NOT GO TO POSITIVE LOCKUP
OUTPUT GOES TO POSITIVE LOCKUP
OUTPUT GOES TO NEGATIVE LOCKUP
OUTPUT DOES NOT GO TO NEGATIVE LOCKUP
13
SECOND STAGE IS OPERATIVE
12
CHECK THE FOLLOWING COMPONENTS:
TRANSISTOR Q5
TRANSISTOR Q6
ASSOCIATED COMPONENTS
OUTPUT IS LOCKED UP NEGATIVE
OUTPUT IS ZERO VOLTS ±250MV
OUTPUT IS LOCKED UP POSITIVE
14
CHECK THE FOLLOWING COMPONENTS:
TRANSISTOR Q5
TRANSISTOR Q6
ASSOCIATED COMPONENTS
15
PROCEED TO BLOCK 18 SHEET 2 OF 2 OF TROUBLESHOOTING GUIDE
16
AMPLIFIER IS OPERATIVE. PROCEED TO PARA.2.4 OF SECTION 2-INITIAL CHECKOUT PROCEDURE
17
PROCEED TO BLOCK 19 SHEET 2 OF 2 OF TROUBLESHOOTING GUIDE III
TROUBLESHOOTING GUIDE III
SHEET 1 OF 2
MODEL 2820-NORMAL MODE AMPLIFIER

OPTION	SCHEMATIC	ASSEMBLY
V1	430603	402303, 402305
V2	430604	402304, 402305
V3	430602	402390, 402305



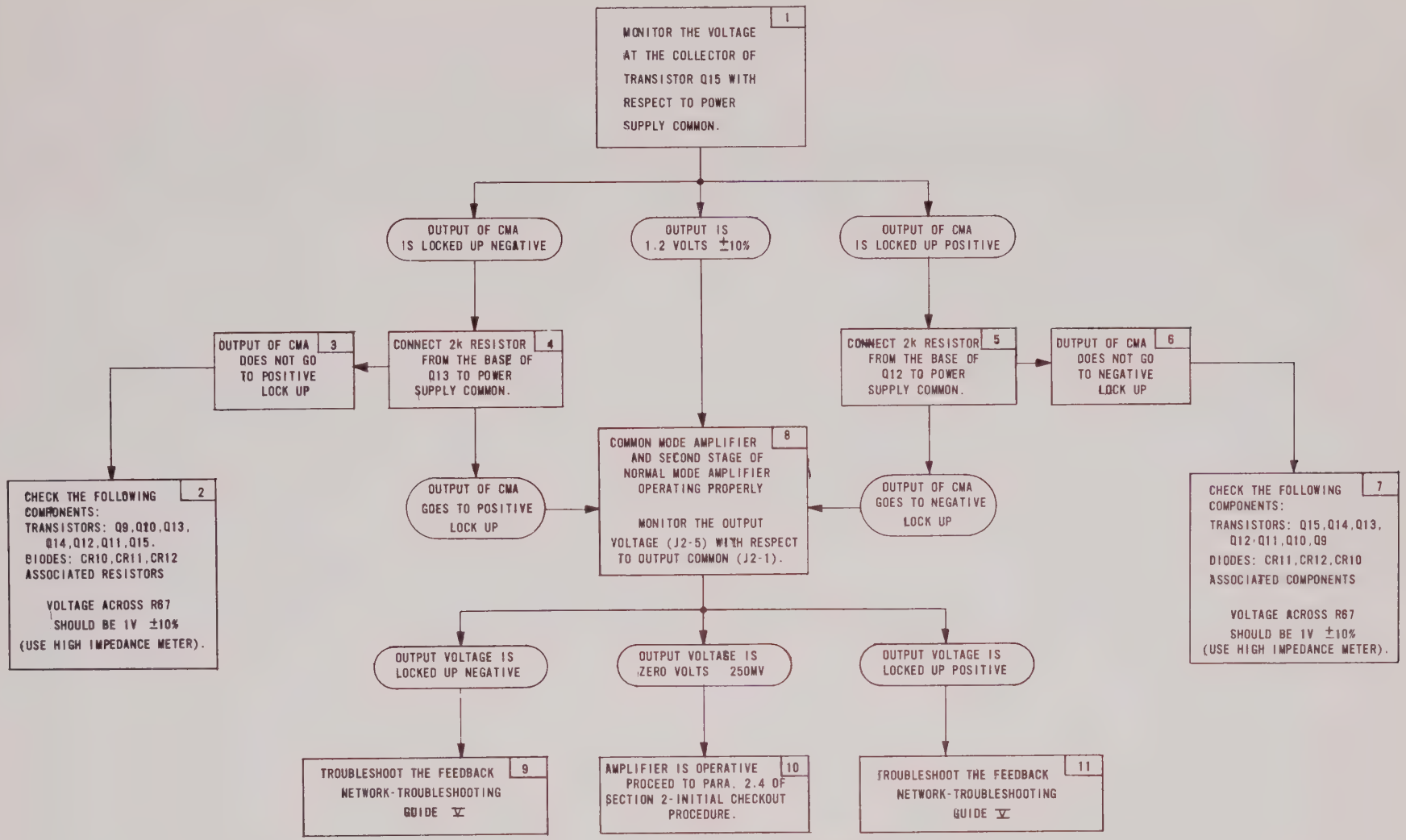
TROUBLESHOOTING GUIDE II
SHEET 1 OF 1
MODEL 2820-100MA OUTPUT AMPLIFIER

OPTION	SCHEMATIC	ASSEMBLY
V1	430603	402303
V2	430604	402304
V3	430602	402390



TROUBLESHOOTING GUIDE I
SHEET 1 OF 1
MODEL 2820- POWER SUPPLY

OPTION	SCHEMATIC	ASSEMBLY
V1	430603	402303
V2	430604	402304
V3	430602	402390

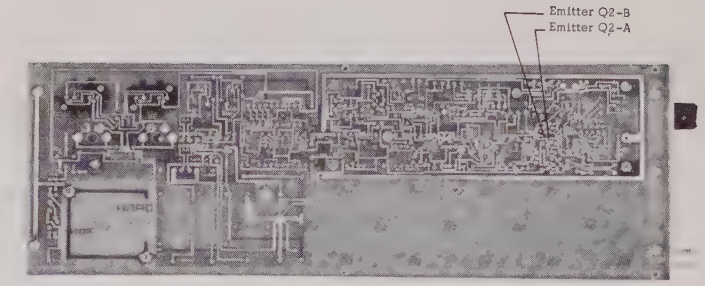

1
MONITOR THE VOLTAGE AT THE COLLECTOR OF TRANSISTOR Q15 WITH RESPECT TO POWER SUPPLY COMMON.
OUTPUT OF CMA IS LOCKED UP NEGATIVE
OUTPUT IS 1.2 VOLTS ±10%
OUTPUT OF CMA IS LOCKED UP POSITIVE
OUTPUT OF CMA DOES NOT GO TO POSITIVE LOCK UP 3
CONNECT 2k RESISTOR FROM THE BASE OF Q13 TO POWER SUPPLY COMMON. 4
CONNECT 2k RESISTOR FROM THE BASE OF Q12 TO POWER SUPPLY COMMON. 5
OUTPUT OF CMA DOES NOT GO TO NEGATIVE LOCK UP 6
CHECK THE FOLLOWING COMPONENTS: 2
TRANSISTORS: Q9,Q10,Q13, Q14,Q12,Q11,Q15.
DIODES: CR10,CR11,CR12
ASSOCIATED RESISTORS
VOLTAGE ACROSS R67 SHOULD BE 1V ±10%
(USE HIGH IMPEDANCE METER).
OUTPUT OF CMA GOES TO POSITIVE LOCK UP
COMMON MODE AMPLIFIER AND SECOND STAGE OF NORMAL MODE AMPLIFIER OPERATING PROPERLY 8
MONITOR THE OUTPUT VOLTAGE (J2-5) WITH RESPECT TO OUTPUT COMMON (J2-1).
OUTPUT OF CMA GOES TO NEGATIVE LOCK UP
CHECK THE FOLLOWING COMPONENTS: 7
TRANSISTORS: Q15,Q14,Q13, Q12,Q11,Q10,Q9
DIODES: CR11,CR12,CR10
ASSOCIATED COMPONENTS
VOLTAGE ACROSS R67 SHOULD BE 1V ±10%
(USE HIGH IMPEDANCE METER).
OUTPUT VOLTAGE IS LOCKED UP NEGATIVE
OUTPUT VOLTAGE IS ZERO VOLTS 250MV
OUTPUT VOLTAGE IS LOCKED UP POSITIVE
TROUBLESHOOT THE FEEDBACK NETWORK-TROUBLESHOOTING GUIDE V 9
AMPLIFIER IS OPERATIVE PROCEED TO PARA. 2.4 OF SECTION 2-INITIAL CHECKOUT PROCEDURE. 10
TROUBLESHOOT THE FEEDBACK NETWORK-TROUBLESHOOTING GUIDE V 11

TROUBLESHOOTING GUIDE IV
SHEET 1 OF 1
MODEL 2820-COMMON MODE AMPLIFIER (CMA)

OPTION	SCHEMATIC	ASSEMBLY
V1	430603	402303
V2	430604	402304
V3	430602	402390

1. REMOVE THE AC POWER FROM THE AMPLIFIER.
FOR V2 OPTION-PLACE THE MULTIPLIER SWITCH TO THE X1 POSITION

2. MEASURE THE RESISTANCE BETWEEN THE EMITTERS OF TRANSISTOR Q2



3. THE RESISTANCE VALUE FOR EACH GAIN POSITION SHOULD BE:

GAIN	RESISTANCE
20	13.50k ±1%
50	5.38k ±1%
100	2.73k ±1%
200	1.37k ±1%
500	.539k ±1%
1000	.275k ±1%

SOME RESISTANCE VALUES, BUT NOT ALL RESISTANCE VALUES ARE OUT OF TOLERANCE

4. CHECK THE GAIN RESISTOR.

GAIN	RESISTOR
50	R15
100	R16
200	R17
500	R18
1000	R19

ALL RESISTANCE MEASUREMENTS ARE OUT OF TOLERANCE

5. CHECK THE RESISTORS IN THE FEEDBACK NETWORK: R20, R24, R21, R23, R26, AND POTENTIOMER R25

CHECK RESISTORS R40, R41, R42, R43, R44, AND R46 CHECK R45 AND R47, THE VALUES OF THESE TWO RESISTORS ARE STAMPED ON THE RESISTOR

RESISTANCE VALUES ARE WITHIN TOLERANCE

6. APPLY THE AC POWER TO THE AMPLIFIER.
PLACE THE GAIN SWITCH TO A HIGH GAIN POSITION(100)
CONNECT THE P-INPUT(J1-8), N-INPUT(J1-4) AND GUARD(J1-7) TO OUTPUT COMMON (J2-1).

OUTPUT IS LOCKED UP POSITIVE OR NEGATIVE

7. MONITOR THE OUTPUT (J2-5) WITH RESPECT TO OUTPUT COMMON(J2-1).

8. MAKE CERTAIN NONE OF THE TROUBLESHOOTING STEPS WERE OVERLOOKED.
RETURN AMPLIFIER TO DANA LABORATORIES ALONG WITH REPAIR/RETURN FORM.

OUTPUT IS ZERO ±250MV

9. PROCEED TO PARA.2.4 OF SECTION 2-INITIAL CHECKOUT PROCEDURE

TROUBLESHOOTING GUIDE V
SHEET 1 OF 1
MODEL 2820-FEEDBACK NETWORK

OPTION	SCHEMATIC	ASSEMBLY
V1	430603	402303
V2	430604	402304
V3	430602	402390

SECTION 7

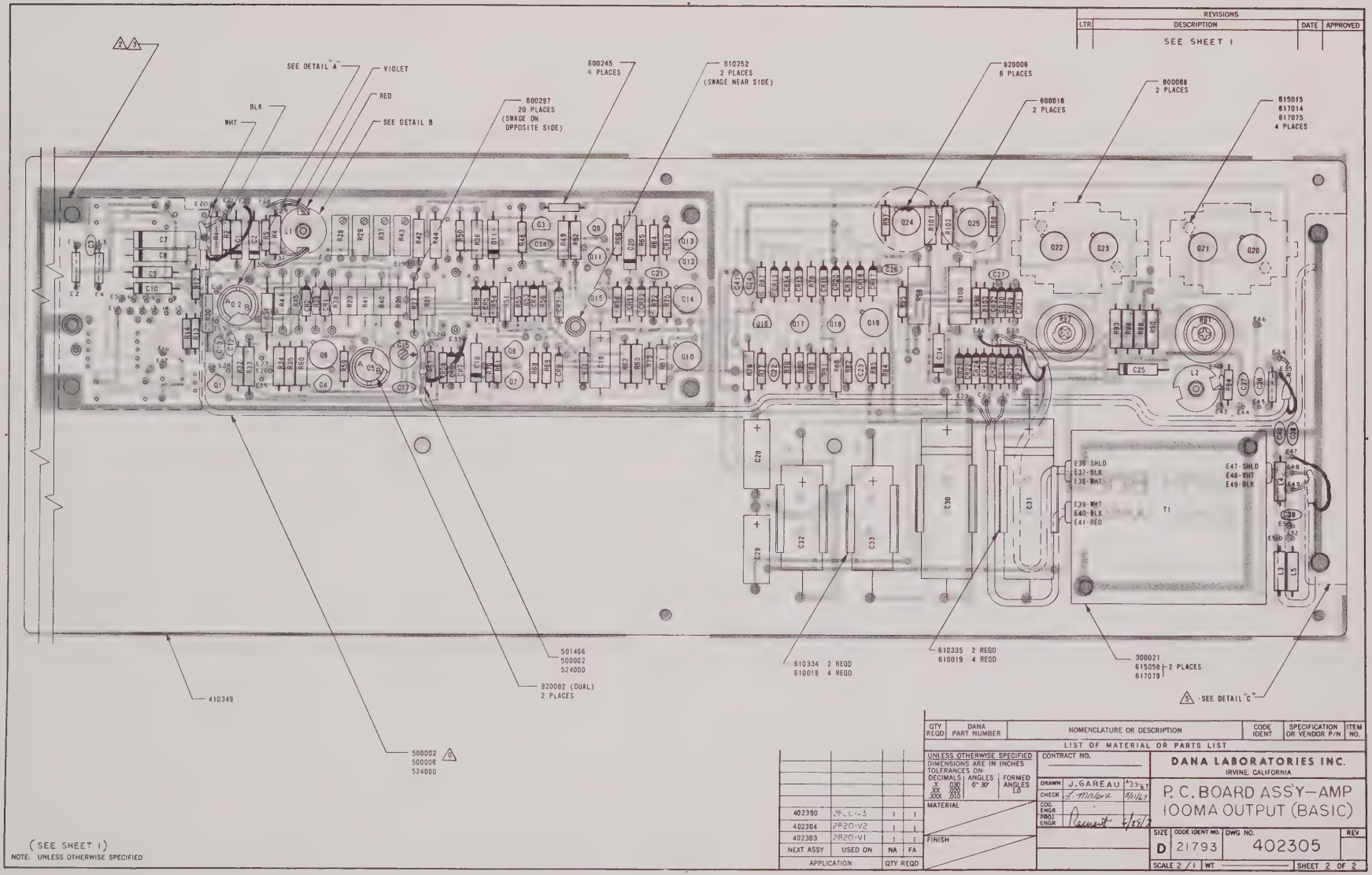
DRAWINGS AND PARTS LISTS

7.1 DRAWINGS

PC Board Assembly - Amp 100MA Output (Basic) (2 of 2)	402305
Schematic - Amplifier 100MA O.O., V1 Option	430603
Schematic - Amplifier 100MA O.P., V2 Option	430604
Schematic - Amplifier 100MA O.P., V3 Option	430602
PC Board Assembly - Amp 100MA Output V1 Option	402303
PC Board Assembly - Amp 100MA Output V2 Option	402304
PC Board Assembly - Amp 100MA Output V3 Option	402390
Outline Dimensional, Amplifier Model 2820	452400
Outline Dimensional, Enclosure Model 2008-1	452402
Outline Dimensional, Enclosure Model 2008-2	452403

7.2 PARTS LISTS

Parts Lists follow the drawings in the same sequence in which the drawings are listed.



LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		

REVISIONS

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
1	402390	PC BD-3	1	1	
1	402304	2R20-V2	1	1	
1	402303	2R20-V1	1	1	
NEXT ASSY	USED ON	NA	FA		
APPLICATION		QTY REQD			

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS X .030 XX .010 XXX .005 | ANGLES 0° 30' | FORMED ANGLES ±1°
MATERIAL
FINISH

CONTRACT NO.

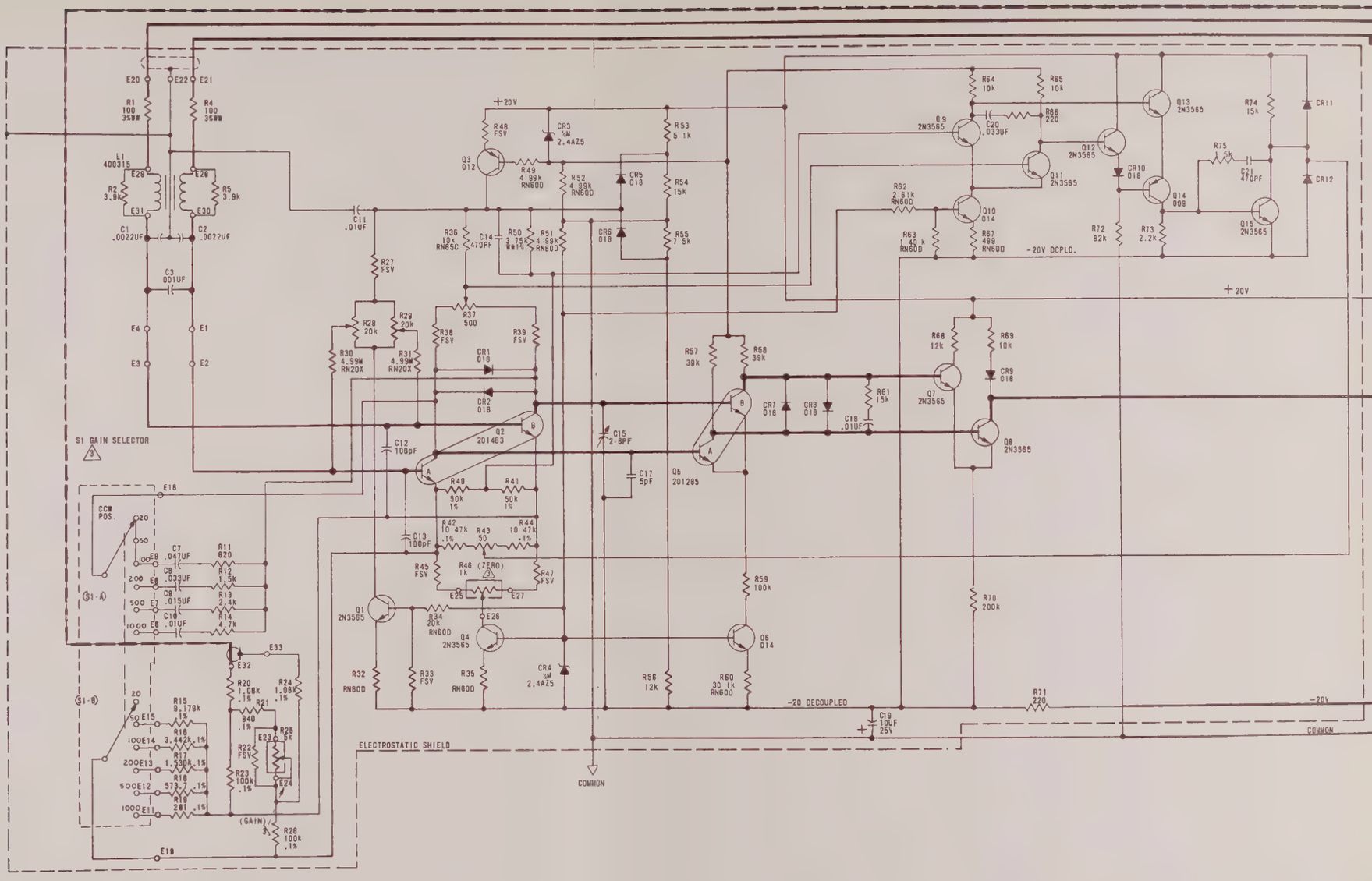
DRAWN J. GAREAU 4/23/67
CHECK [signature] 5/11/67
COG ENGR
PROJ ENGR [signature] 6/15/67

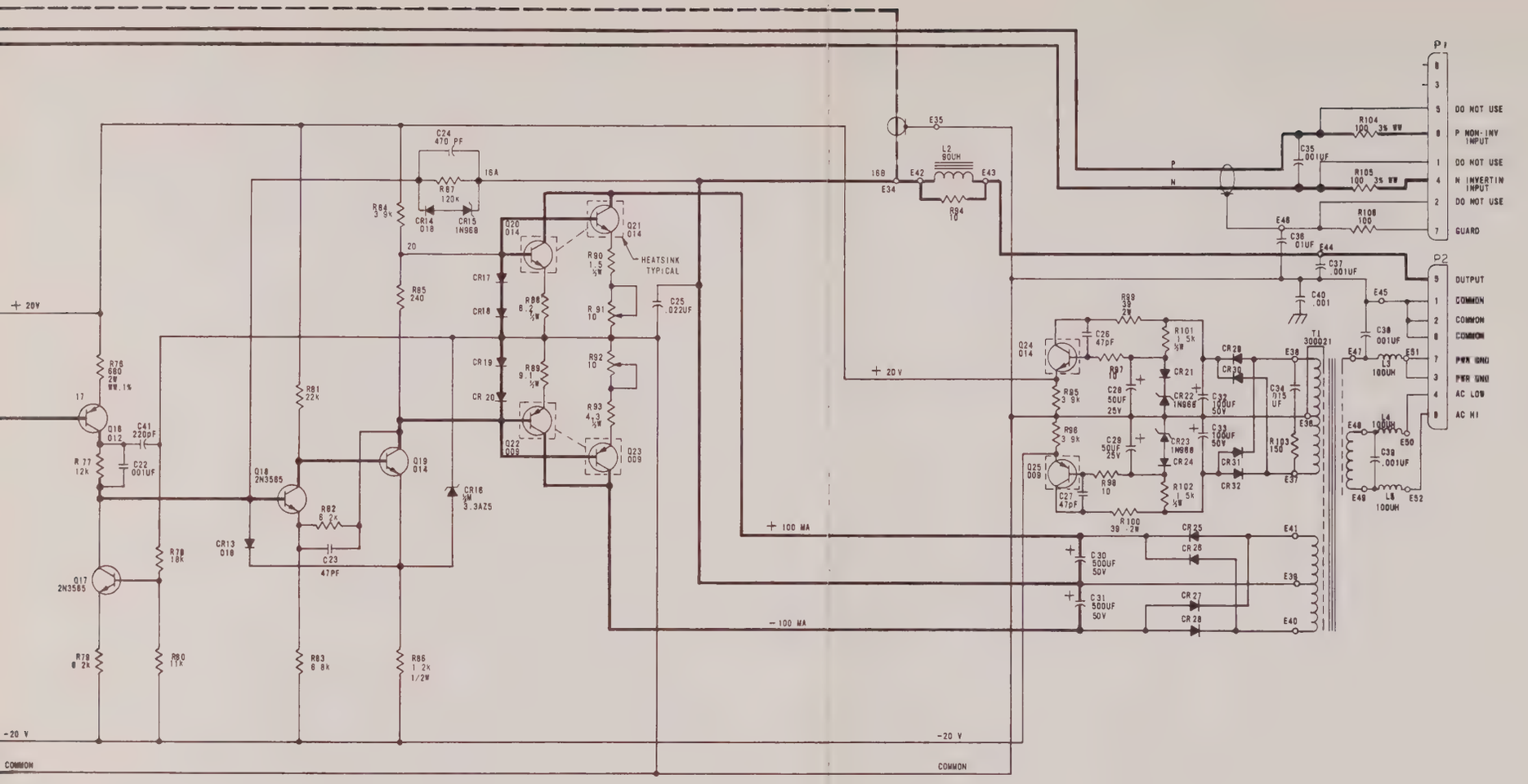
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P. C. BOARD ASSY—AMP 100MA OUTPUT (BASIC)

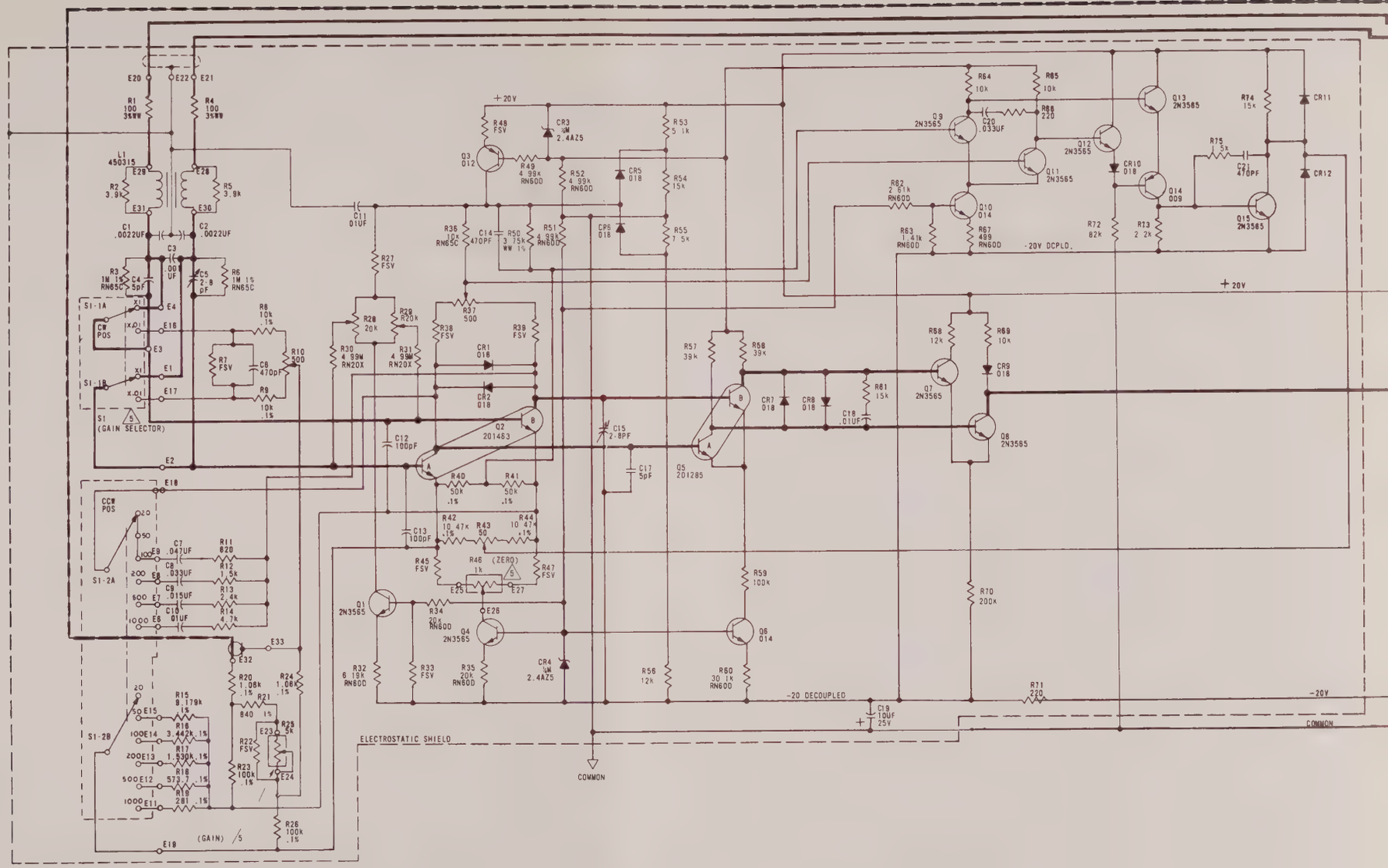
SIZE D | CODE IDENT NO. 21793 | DWG NO. 402305 | REV
SCALE 2/1 | WT | SHEET 2 OF 2

(SEE SHEET 1)
NOTE: UNLESS OTHERWISE SPECIFIED


S1 GAIN SELECTOR
ELECTROSTATIC SHIELD
COMMON
-20 DECOUPLED
-20V DCPLD.
+20V
-20V
CCW POS.
(S1-A)
(S1-B)
(GAIN)
L1 400315
Q1 2N3565
Q2 201483
Q3 012
Q4 2N3565
Q5 201285
Q6 014
Q7 2N3565
Q8 2N3565
Q9 2N3565
Q10 014
Q11 2N3565
Q12 2N3565
Q13 2N3565
Q14 009
Q15 2N3565



CONTRACT NO.		DANA LABORATORIES INC. IRVINE, CALIFORNIA
NAME	DATE	SCHEMATIC — AMPLIFIER, 100 MA O.P., V1 OPTION
DR A CHAUSSE		
CHK		
APPD	6/19/67	
SIZE D	CODE IDENT NO. 21793	DWG NO. 430603
SCALE —	WT —	SHEET 1 OF 2


+20V
-20V DCPLD.
-20 DECOUPLED
-20V
COMMON
ELECTROSTATIC SHIELD
(GAIN) /5
S1 (GAIN SELECTOR)
S1-1A
S1-1B
S1-2A
S1-2B
CW POS
CCW POS
Q1 2N3565
Q2 201483
Q3 012
Q4 2N3565
Q5 201285
Q6 014
Q7 2N3565
Q8 2N3565
Q9 2N3565
Q10 014
Q11 2N3565
Q12 2N3565
Q13 2N3565
Q14 009
Q15 2N3565
CR1 018
CR2 018
CR3 1W 2.4AZ5
CR4 1W 4AZ5
CR5 018
CR6 018
CR7 018
CR8 018
CR9 018
CR10 018
CR11
CR12
C1 .0022UF
C2 .0022UF
C3 .001 UF
C4 5pF
C5 2-8 pF
C7 .047UF
C8 .033UF
C9 .015UF
C10 01UF
C11 01UF
C12 100pF
C13 100pF
C14 470PF
C15 2-8PF
C17 5pF
C18 .01UF
C19 10UF 25V
C20 .033UF
C21 470PF
R1 100 3%W
R2 3.9k
R3 1M 1% RN65C
R4 100 3%W
R5 3.9k
R6 1M 1% RN65C
R7 FSV
R8 10k .1%
R9 10k .1%
R10 500
R11 820
R12 5.5k
R13 2.4k
R14 4.7k
R15 8.179k .1%
R16 3.442k .1%
R17 1.530k .1%
R18 573.7 .1%
R19 281 .1%
R20 1.08k .1%
R21 840 1%
R22 FSV
R23 100k .1%
R24 1.08k .1%
R25 5k
R26 100k .1%
R27 FSV
R28 20k
R29 R20k
R30 4.99k RN20X
R31 4.99k RN20X
R32 6.19K RN60D
R33 FSV
R34 20k RN60D
R35 20k RN60D
R36 10k RN65C
R37 500
R38 FSV
R39 FSV
R40 50k .1%
R41 50k .1%
R42 10.47k .1%
R43 50
R44 10.47k .1%
R45 FSV
R46 (ZERO) 1k
R47 FSV
R48 FSV
R49 4.99k RN60D
R50 3.75k WW 1%
R51 4.99k RN60D
R52 4.99k RN60D
R53 5.1k
R54 15k
R55 7.5k
R56 12k
R57 39k
R58 39k
R59 100k
R60 30.1k RN60D
R61 15k
R62 2.61k RN60D
R63 1.41k RN60D
R64 10k
R65 10k
R66 220
R67 499 RN60D
R68 12k
R69 10k
R70 200k
R71 220
R72 82k
R73 2.2k
R74 15k
R75 5k
E1
E2
E3
E4
E8
E10
E11
E12
E13
E14
E15
E16
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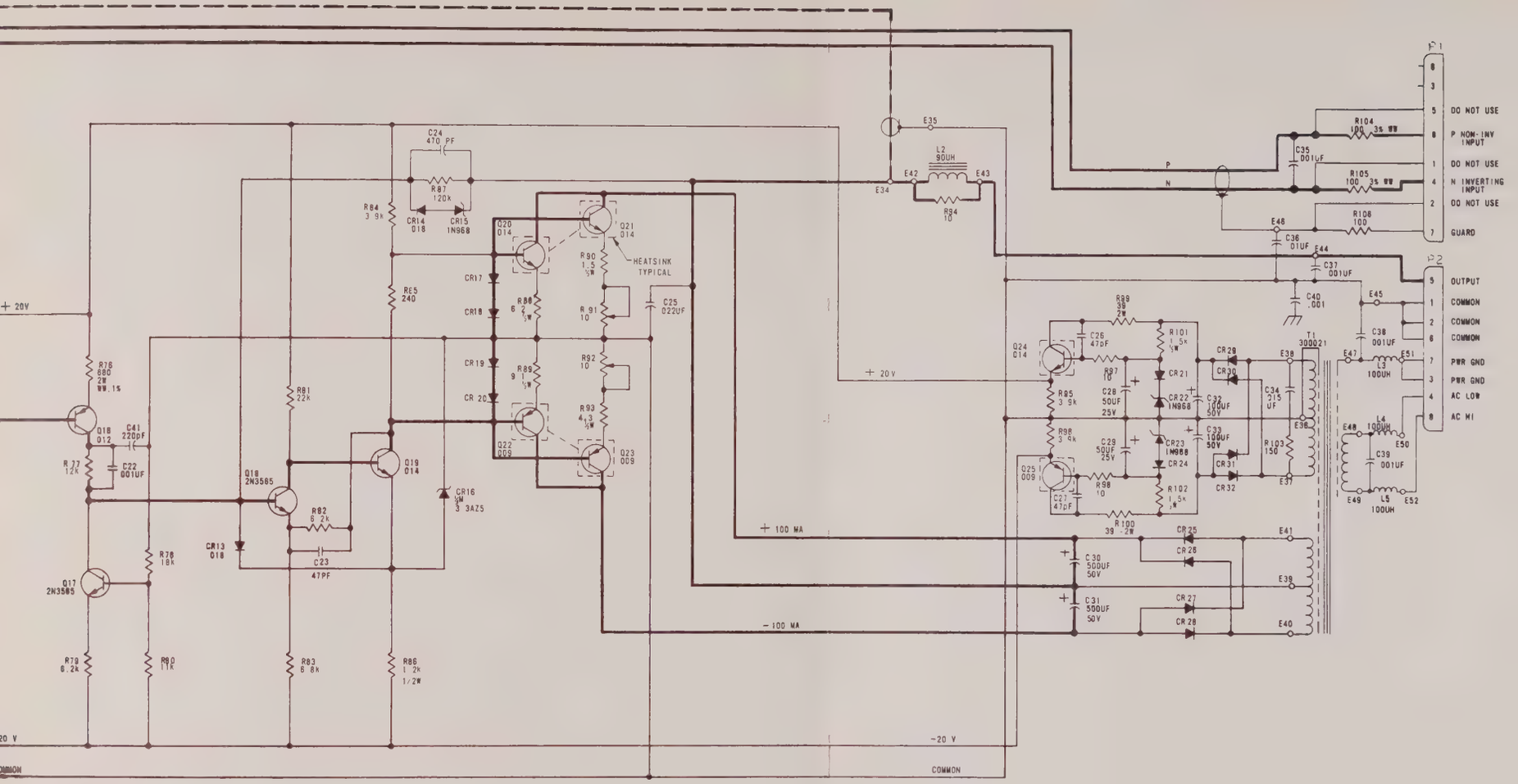
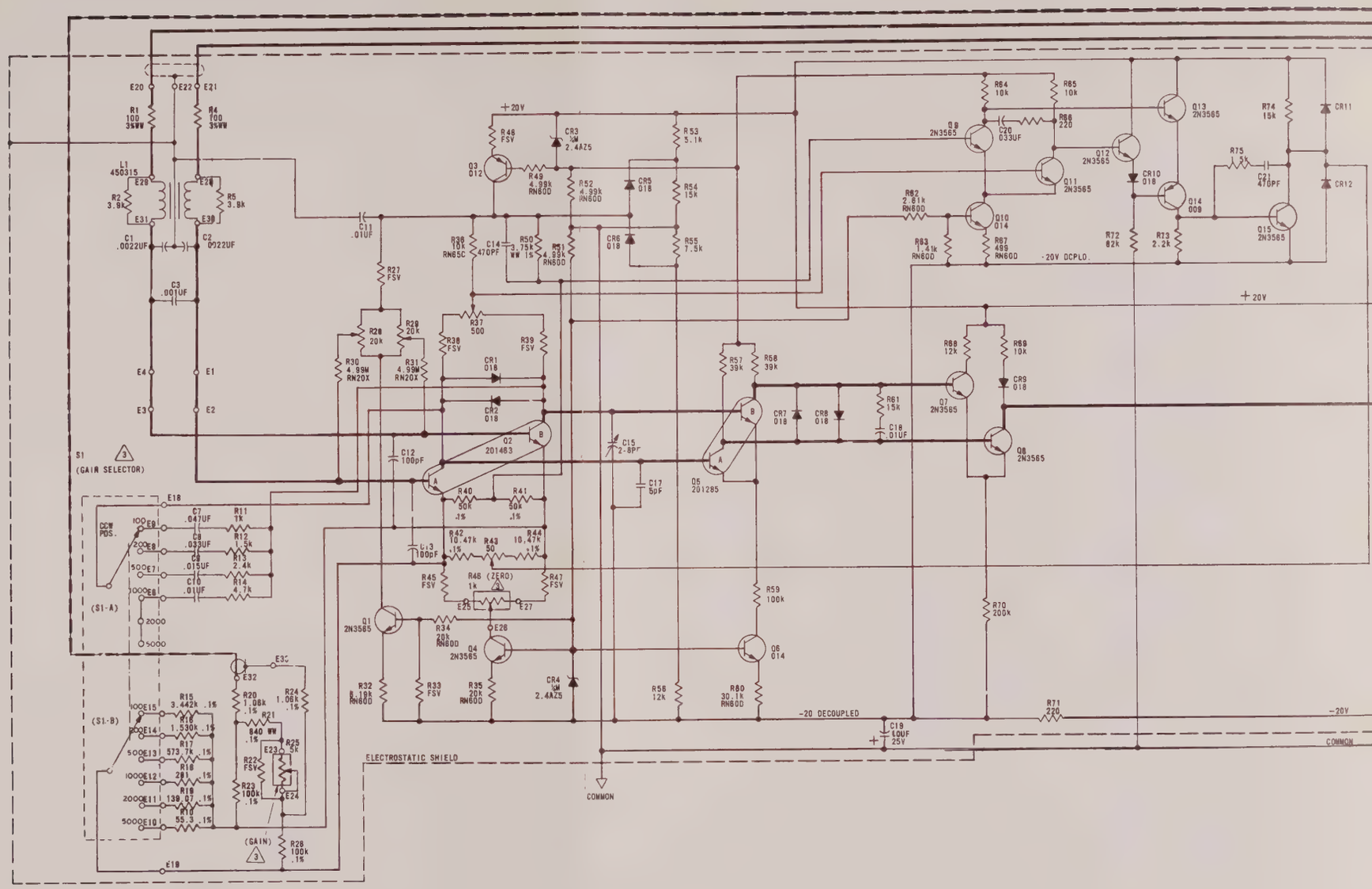
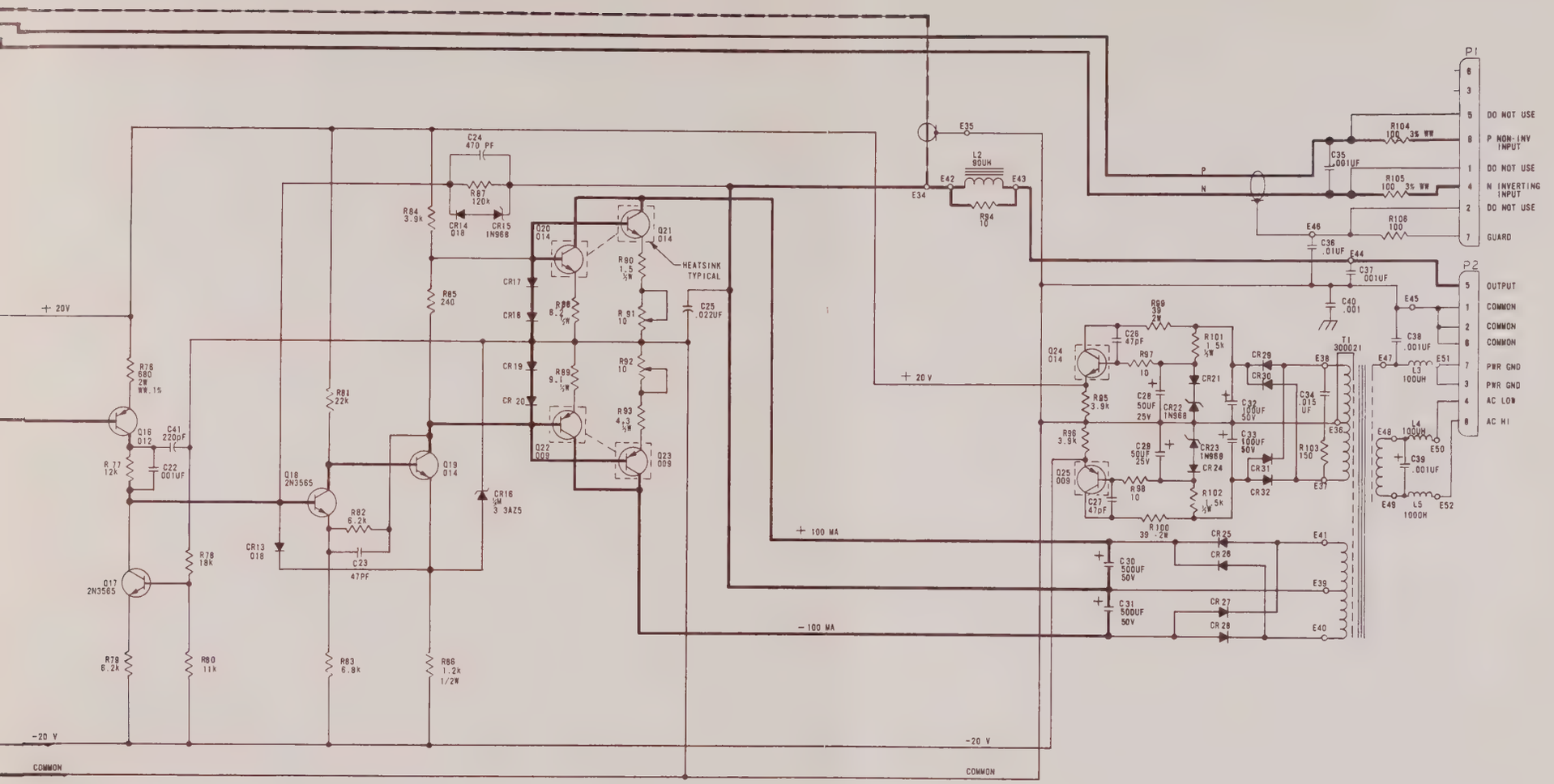
E32
E33

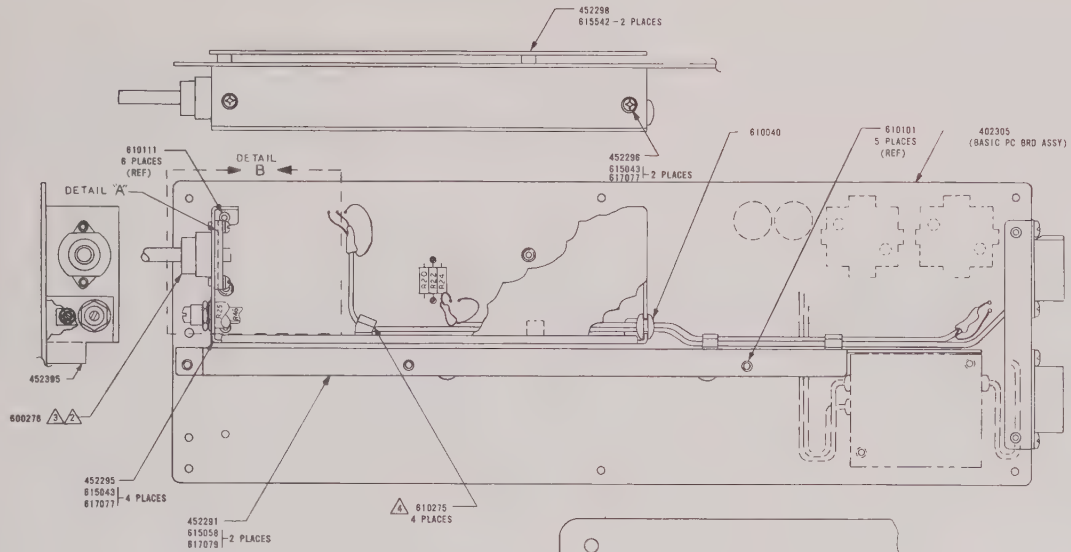


CONTRACT NO.		DANA LABORATORIES INC. IRVINE, CALIFORNIA	
NAME	DATE	SCHEMATIC — AMPLIFIER, 100 MA O.P., V2 OPTION	
DR A CHAUSSEE	5-17-67		
CHK J APPROVE	5-18-67		
APPD Clement	6/19/67		
		SIZE D	CODE IDENT NO. 21793
		DWG NO. 430604	
		SCALE —	WT —
		SHEET 1 OF 2	


E20
E22
E21
R1 100 3%WW
R4 100 3%WW
L1 450315
E29
E28
E30
E31
E39
R2 3.9k
R5 3.9k
C1 .0022UF
C2 .0022UF
C3 .001UF
E4
E1
E3
E2
S1
(GAIN SELECTOR)
E18
CCW POS.
100 E9
200 E8
500 E7
1000 E6
2000
5000
C7 .047UF
C8 .033UF
C9 .015UF
C10 .01UF
R11 1k
R12 1.5k
R13 2.4k
R14 4.7k
(S1-A)
(S1-B)
E32
E33
R15 3.442k .1%
R16 1.530k .1%
R17 573.7k .1%
R18 281 1%
R19 139.07 .1%
R10 55.3 .1%
R20 1.06k .1%
R21 840 WW .1%
R22 FSV
R23 100k .1%
R24 1.06k .1%
R25 5k
E23
E24
(GAIN)
R28 100k .1%
E19
C11 .01UF
R27 FSV
R29 20k
R30 4.99M RN20X
R31 4.99M RN20X
+20V
R46 FSV
CR3 2.4AZ5
Q3 O12
R49 4.99k RN60D
R52 4.99k RN60D
R53 5.1k
CR5 O18
R54 15k
R36 10k RN65C
C14 470PF
R50 3.75k WW .1%
R51 4.99k RN60D
CR6 O18
R55 7.5k
R28 20k
R37 500
R38 FSV
R39 FSV
CR1 O18
CR2 O18
Q2 2N1483
C12 100pF
C15 2-8PF
C17 5pF
R40 50k .1%
R41 50k .1%
C13 100pF
R42 10.47k .1%
R43 50 .1%
R44 10.47k .1%
R45 FSV
R48 (ZERO) 1k
R47 FSV
E25
E27
E26
Q1 2N3565
R34 20k RN60D
Q4 2N3565
R32 8.19k RN60D
R33 FSV
R35 20k RN60D
CR4 2.4AZ5
R57 39k
R58 39k
Q5 2N1285
CR7 O18
CR8 O18
R61 15k
C18 .01UF
R59 100k
R56 12k
R60 30.1k RN60D
R64 10k
R65 10k
Q9 2N3565
C20 .033UF
Q12 2N3565
Q11 2N3565
R62 2.61k RN60D
Q10 O14
R63 1.41k RN60D
R67 499 RN60D
-20V DCPLD.
CR10 O18
Q13 2N3565
Q14 O09
R72 82k
R73 2.2k
R75 1k
C21 470PF
Q15 2N3565
R74 15k
CR11
CR12
+20V
R68 12k
R69 10k
CR9 O18
Q7 2N3565
Q8 2N3565
R70 200k
Q6 O14
-20 DECOUPLED
C19 10UF 25V
R71 220
-20V
COMMON
ELECTROSTATIC SHIELD
COMMON

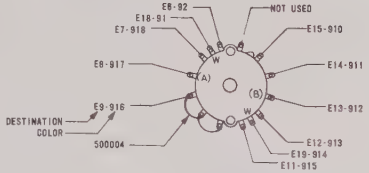


CONTRACT NO.		DANA LABORATORIES INC. IRVINE, CALIFORNIA	
NAME	DATE	SCHEMATIC — AMPLIFIER, 100 MA O.P., V3 OPTION	
DR A CHAUSSEE	4-24-67		
CHK	5-4-67		
APPD	6/9/67		
		SIZE D	CODE IDENT NO. 21793
		DWG NO. 430602	
		SCALE —	WT —
		SHEET 1 OF 2	

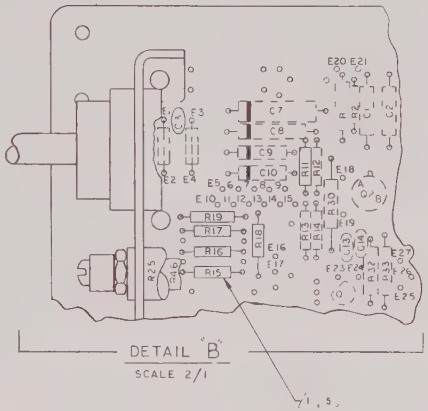


REF DES	PART NO	DESCRIPTION
R46	040020	1k POT
R25		FSV GAIN
R24	402156	VERNIER
R20		ASSEMBLY
R22	402156	FSV GAIN
R19	020130	28I WW 1%
R18	020081	573.7 WW 1%
R17	020082	1 530k WW 1%
R16	020083	3 442k WW ½
R15	020084	9 179k WW 1%
R11	000621	62 1/4W 5%

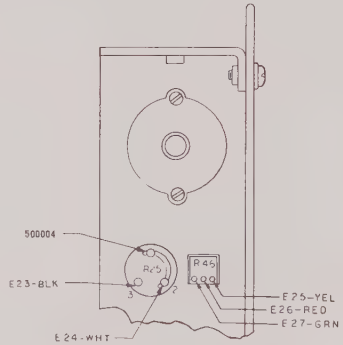
1



DETAIL "A"
(VIEWED FROM FRONT)



DETAIL "B"
SCALE 2/1



NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE SCHEMATIC: 430803.
2. COMPONENTS IN PHANTOM LINES SHOWN FOR REFERENCE ONLY.
3. ROUTE CABLE AS SHOWN - CLAMP TO BRACKETS AS REQUIRED.
4. COAT AREA WITH HUMI-SEAL AS REQUIRED AVOIDING BRACKET MOUNTING HOLES. MOUNT BRACKET TO PC BOARD.
5. MOUNT SWITCH R25 & R46 TO BRACKET WIRE PER DETAIL A WIRING ON SWITCH SHOULD ROLL OFF ONE SIDE, KEEPING WIRE LENGTH TO A MINIMUM
6. ADD OPTIONAL COMPONENTS PER DANA WORKMANSHIP STANDARDS.

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

NEXT ASSY	USED ON	NA	FA
402300	2820-V1	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: X .030, XX .005, XXX .010
ANGLES 0° 30'
FORMED ANGLES 1.0
MATERIAL
FINISH

CONTRACT NO.

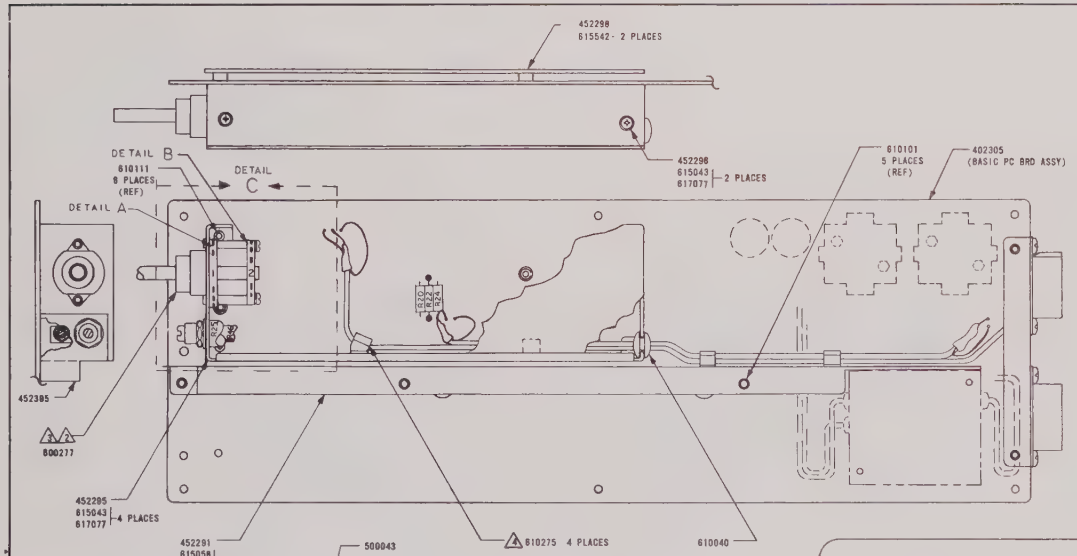
DRAWN J. GAREAU 4-4-1967
CHECK 5-5-67
COG ENGR
PROJ ENGR

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSY-AMP, 100 MA OUTPUT V1 OPTION

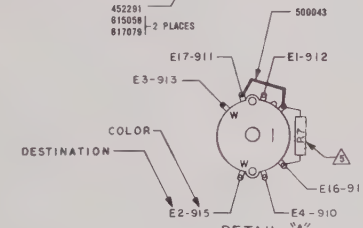
SIZE	CODE IDENT NO	DWG NO	REV
D	21793	402303	

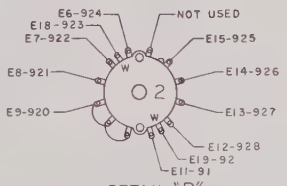
SCALE 1/1 | WT | SHEET 1 OF 1



R46	040020	1k POT
R25		FSV GAIN
R24	402156	VERNIER
R20		ASSEMBLY
R22	402158	FSV GAIN
R19	020130	281 OHMS WW 1%
R18	020081	573.7 OHMS 22 1%
R17	020082	1.530k WW .1%
R16	020083	3.442k WW .1%
R15	020084	9.179k WW .1%
R11	000621	820 OHMS 1/4W 5%
R10	040071	500 OHMS POT
R9	020097	10k WW .1%
R8	020097	10k WW .1%
R7	010176	FSV 1W-2W 1%
R6	010111	1W 1% MFRN65C
R3	010111	1W 1% MFRN65C
C6	101641	470 pF DISC
C5	130004	2-8 pF VARIBLE
C4	100009	5 pF DISC

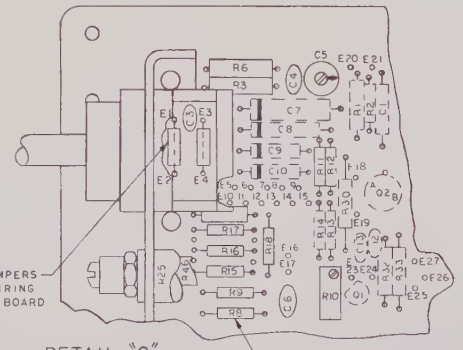
REF DES	PART NO	DESCRIPTION

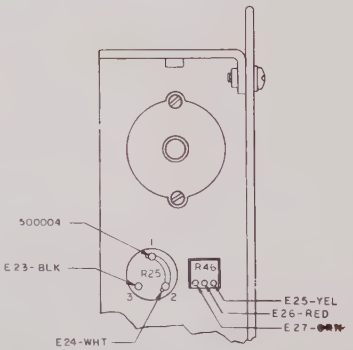




ATTENUATOR SWITCH WIRING

(VIEWED FROM FRONT)





7. REFERENCE SCHEMATIC: 430604

6. COMPONENTS IN PHANTOM LINES SHOWN FOR REFERENCE ONLY.

5. R7 (FSV) TO BE ADDED AS PART OF FINAL CHECKOUT-CALIBRATION.

4. ROUTE CABLE AS SHOWN - CLAMP TO BRACKETS AS REQUIRED

3. COAT AREA WITH HUMI-SEAL AS REQ'D AVOIDING BRACKET MOUNTING HOLES. MOUNT BRACKET TO PC BOARD.

2. MOUNT SWITCH, R25 & R46 TO BRACKET-WIRE PER DETAIL "A"-WIRING ON SWITCH SHOULD ROLL OFF ONE SIDE, KEEPING WIRE LENGTH TO A MINIMUM.

1. ADD OPTIONAL COMPONENTS PER DANA WORKMANSHIP STANDARDS.

NOTE: UNLESS OTHERWISE SPECIFIED

402301	2820-V2	1	1
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P N	ITEM NO

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS: X .030, XX .000, XXX .010
ANGLES 0° 30'
FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO. — —

DRAWN HM AREA 1-3-7

CHECK

COG ENGR

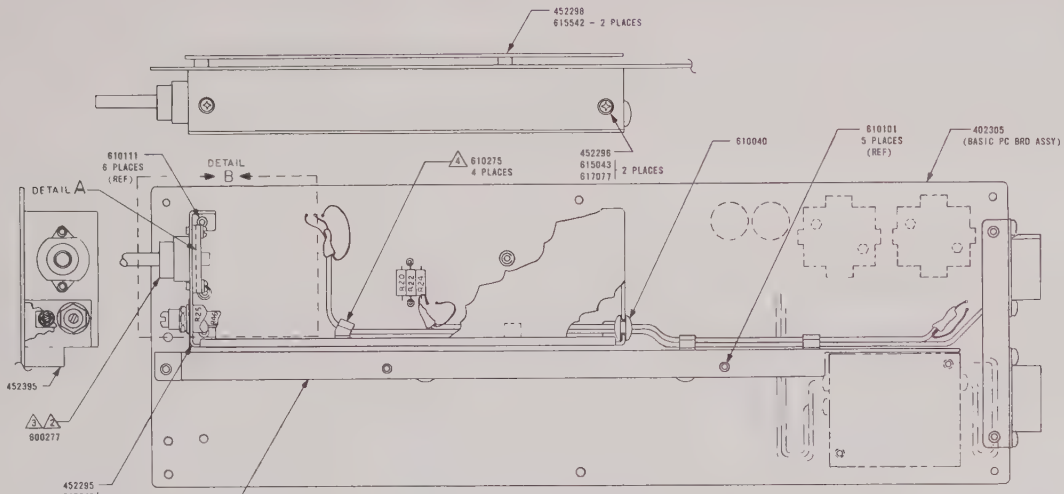
PROJ ENGR

DANA LABORATORIES INC.
IRVINE CALIFORNIA

P.C. BOARD ASSY - AMP, 100 MA OUTPUT V2 OPTION

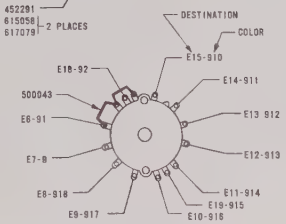
SIZE	CODE IDENT NO	DWG NO	REV
D	21793	402304	

SCALE 1/1 | WT — — — | SHEET 1 OF 1

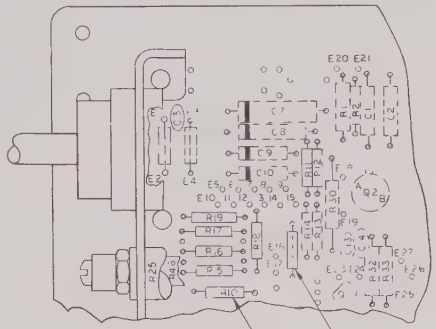


R48	040020	1K POT
R25		FSV GAIN
R24	402158	VERNIER
R20		ASSEMBLY
R22	402158	FSV GAIN
R19	020367	139.07 WW .1%
R18	020130	281 WW .1%
R17	020081	573.7 WW .1%
R16	020082	1 530 k WW .1%
R15	020083	3.442 k WW .1%
R11	000102	1 k 1/4W, 5%
R10	020389	55.3 WW .1%
REF DES	PART NO	DESCRIPTION

△1

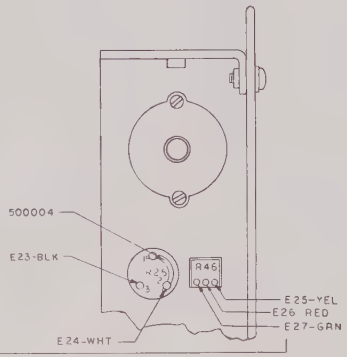


DETAIL "A"
(VIEWED FROM FRONT)



DETAIL "B"
SCALE 2/1

△5



8. REFERENCE: SCHEMATIC 430802

△5 COMPONENTS IN PHANTOM LINES SHOWN FOR REFERENCE ONLY

△4 ROUTE CABLE AS SHOWN. CLAMP TO BRACKETS AS REQUIRED

△3 COAT AREA WITH HUMI-SEAL AS REQUIRED AVOIDING BRACKET MOUNTING HOLES. MOUNT BRACKET TO PC BOARD

△2 MOUNT SWITCH, R25 & R48 TO BRACKET-WIRE PER DETAIL "A". WIRING ON SWITCH SHOULD ROLL OFF ONE SIDE, KEEPING WIRE LENGTH TO A MINIMUM

△1 ADD OPTIONAL COMPONENTS PER DANA WORKMANSHIP STANDARDS

NOTE: UNLESS OTHERWISE SPECIFIED

402389	2820 V3	1	1
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE DENT	SPECIFICATION OR VENDOR P N	ITEM NO

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON- DECIMALS X .030 XX .000 XXX .010 | ANGLES 0° 30' | FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO.

DRAWN BM AREAL 1-13-72

CHECK Roger Mabrey 5-19-72

COG ENGR

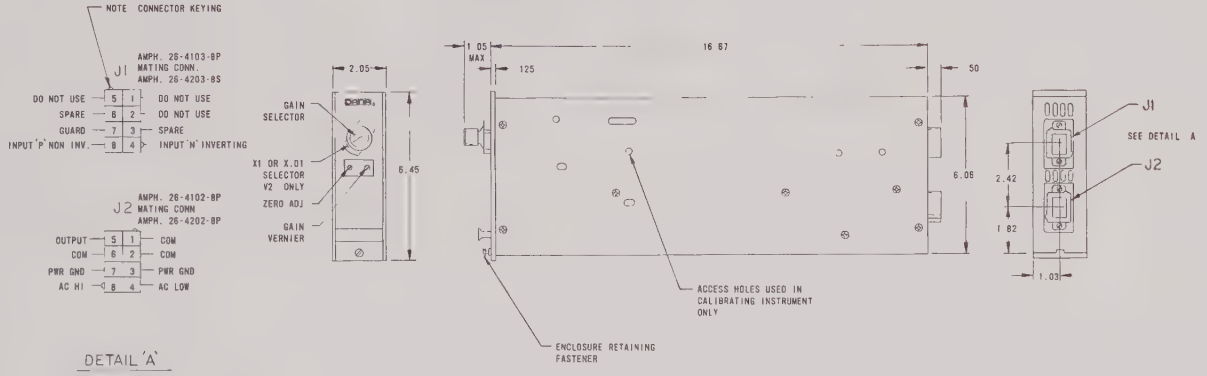
PROJ ENGR Dennis 6/19/72

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSY-AMP, 100MA OUTPUT V3 OPTION

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	402390	

SCALE 1/1 WT SHEET 1 OF 1



DETAIL 'A'

WIRING TYPICAL OF DANA CORD SET NO 402468 AND DANA MODEL 2008-1 & 2008-2 ENCLOSURE

1. OUTLINE TYPICAL FOR 2820 OPTIONS V1, V2, & V3.

NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			
402389	2820 V3		REF	REF	
402301	2820 V2		REF	REF	
402300	2820 V1		REF	REF	
NEXT ASSY	USED ON		NA	FA	
APPLICATION			QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS X .030, XX .020, XXX .010; ANGLES 0° 30'; FORMED ANGLES 1.0

CONTRACT NO.

MATERIAL

FINISH

DRAWN G WILSON 6/21/67

CHECK

COG ENGR

PROJ ENGR

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

OUTLINE DIMENSIONAL
AMPLIFIER MODEL 2820

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	452400	

SCALE 1/2 WT SHEET 1 OF 1

DANA

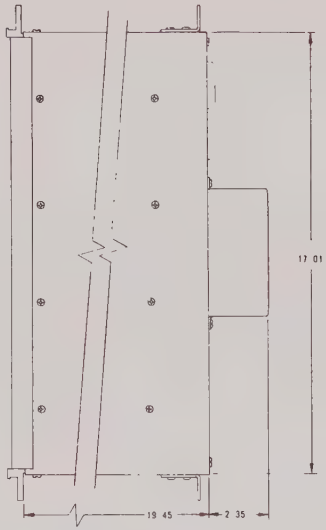
CHANGE NOTICE

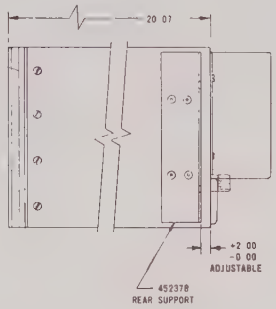
Model 2820 Amplifier
Assembly 452400 Schematic

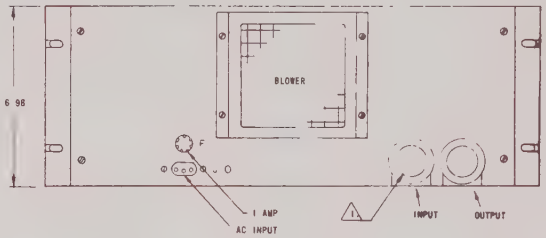
Change part number of J1 to Amphenol 26-4101-8P.

Change part number of mating connector to Amphenol 26-4201-8S.

Change part number of J2 mating connector to Amphenol 26-4202-8S.







QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS X .030, XX .010, XXX .005; ANGLES 0° 30'; FORMED ANGLES ±1°

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN G WILSON 6/22/67
CHECK
COG ENGR
PROJ ENGR

MATERIAL

FINISH

OUTLINE DIMENSIONAL
ENCLOSURE
MODEL 2808-1

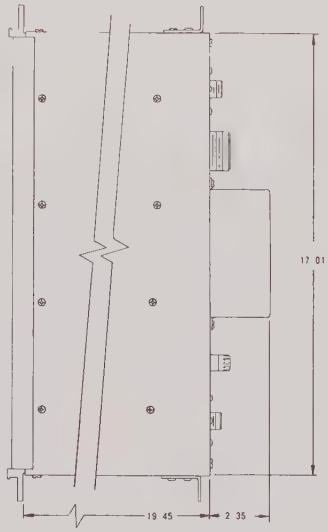
SIZE D | CODE IDENT NO. 21793 | DWG NO. 452402

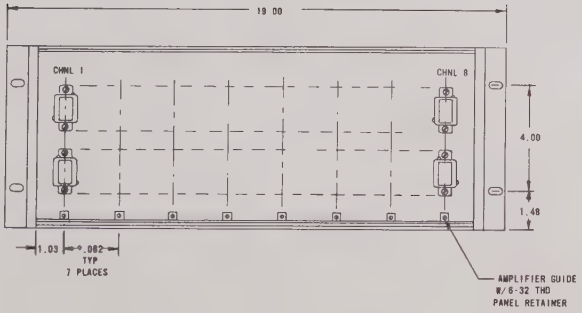
SCALE 1/2 | WT | SHEET 1 OF 2

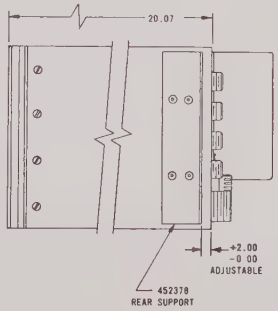
402368	2BO-	REF	REF
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

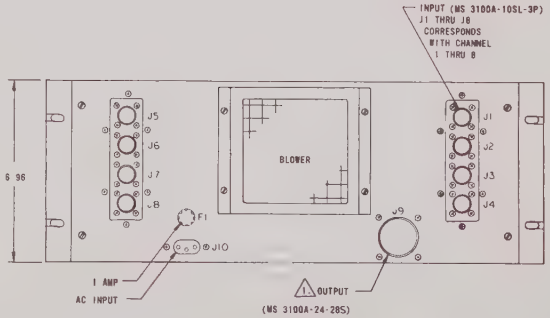
⚠1 ENCLOSURE WIRING PER DANA DRAWING # 430590.

NOTE: UNLESS OTHERWISE SPECIFIED









QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

402371	2808-2	REF	REF
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS: X .030, XX .000, XXX .010 | ANGLES 0° 30' | FORMED ANGLES ±.0

MATERIAL

FINISH

CONTRACT NO.

DRAWN	G WILSON	6/26/67
CHECK	W.F. Schilling	27 JUNE 67
COG. ENGR		6/29/67
PROJ ENGR		6/29/67

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

OUTLINE DIMENSIONAL ENCLOSURE MODEL 2808-2

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	452403	

SCALE 1/2 | WT | SHEET 1 OF 1

⚠ ENCLOSURE WIRING PER DANA DRAWING # 430581.

NOTE: UNLESS OTHERWISE SPECIFIED

APPENDIX A

OPERATING CHARACTERISTICS AND DEFINITIONS

1.0 INTRODUCTION

Tabulated specifications provide a concise, quantitative means for relating an instrument to a potential application. It is also a means for comparing the relative suitabilities of competitive instruments for a given application.

However, an abbreviated description such as this must be used cautiously. Developments in the electronic industry are so rapid that terminology, test conditions, etc., are neither standardized nor binding. Consequently, different manufacturers and different users often apply the same term in different ways, or use different terms to describe the same quantity.

Dana Laboratories adheres to generally recognized standards when they are applicable. However, there are many test procedures and parameters that are neither standard nor well defined. The purpose of the following commentary is to convey to the user the exact meaning of the terms used by Dana in the design, manufacturing and testing of Dana Data Amplifiers.

2.0 DEFINITION OF TERMS

2.1 OUTPUT

Dana Amplifier output is defined as the voltage between the OUTPUT and COMMON terminals. Since both terminals are isolated from the amplifier chassis and power line ground, it is necessary to define the COMMON terminal as the reference point for all voltage measurements. This point is common both to the output and to the internal shielded power supplies.

For specified performance, the COMMON terminal of the amplifier should be connected to the low side of the load. Since many output devices have poorly shielded power supplies, it is often desirable to return this point to ground.

The full scale output of the amplifier is -10 volts to +10 volts DC, peak AC or any combination, at frequencies up to 20 kHz with full rated load. Specifications such as gain accuracy, linearity, and output impedance apply to outputs within this full scale limit. At frequencies from DC to 20 kHz, there is a nominal overscale capability of 20%. Lower output levels may be used beyond 20 kHz.

If a low resistance load, such as a recording galvanometer with a typical 25-ohm resistance, is to be driven, series resistance should be added so that the full scale of the recording instrument corresponds with amplifier full scale. This increases the accuracy of the instrumentation system and also serves to protect the recording instrument from damaging overload. Should the load require a particular driving resistance, such as an external damping resistance, a simple two-resistor network is needed between the amplifier and the load (see Figure 1).

2.2 GAIN

Unless otherwise specified, the term "gain" means the ratio of the magnitude of ΔV_o divided by the magnitude of ΔV_i, where V_o is the output signal and V_i is the input.

Linearity is so great that gain is essentially independent of V_o. Since the Dana unit is a negative feedback amplifier, the gain is determined almost entirely by the ratio of resistors in the feedback network. The specifications are valid for any gain from 20 to 1,000. A small degradation occurs in the 1,000 to 2,500 span. Considerable latitude exists in the number and value of gain steps that can be supplied between the limits of 20 and 2,500.

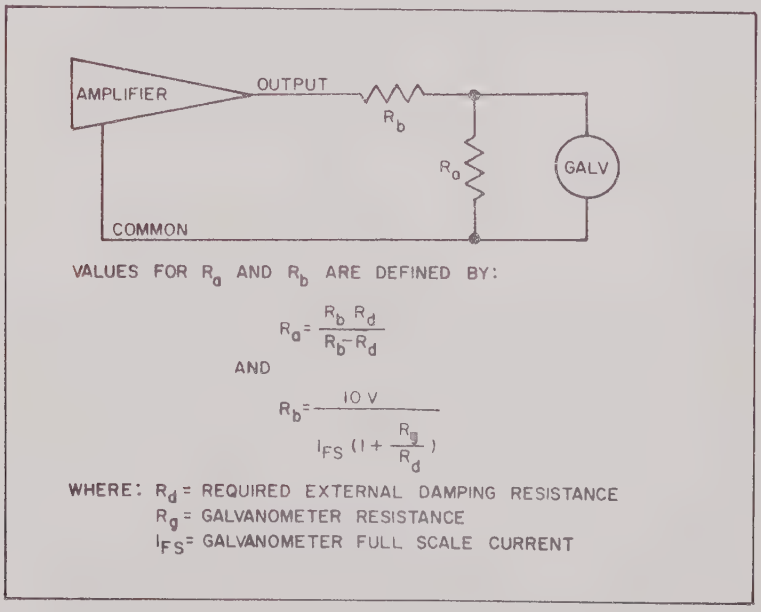


Figure 1 - Two-Resistor Network for Damping Galvanometer

Gain Option V1 provides a continuously variable gain from 20 to 2,500 in six ranges: 20-50, 50-100, 100-200, 200-500, 500-1000, 1000-2500, with a slight overlap between ranges. The resolution and mechanical stability of the continuously variable control limits the gain resolution of the amplifier to $\pm$0.1%. However Option V1 is particularly useful for applications where the load has a limited dynamic range, as in the case of magnetic tape recorders or recording oscillographs. In these applications, it is desirable to match the full scale of the transducer to that of the recorder. This requires either a very large number of closely spaced gain steps or a continuously adjustable gain. At the same time, the limited dynamic range makes it impossible to detect errors in the order of 0.1%. Because this vernier varies the feedback ratio in the amplifier, the frequency response is reduced at the clockwise (high gain) end of the span. Gain stability is $\pm$0.02% with the vernier at its low end.

Gain Option V2 is identical to V1 except that a 100:1 input divider may be selected by a front panel control. This control is concentric to the main gain selector and has two positions with the legends X1 and X0.01.

Procedures for measuring DC and AC gain are included in Section 5, paragraphs 5.4.1 and 5.4.3, respectively.

2.3 LINEARITY

Ideally, gain should be independent of the magnitude of the output voltage from minus full scale to plus full scale. Since the Dana Amplifier's departure from this ideal is so small, the null balance method of measurement is used. Procedures for measuring linearity are included in Section 5, paragraph 5.4.2.

2.4 HIGH FREQUENCY LINEARITY

All amplifiers have inherent nonlinearities which are reduced by negative feedback. Since the feedback ratio decreases at higher frequencies, nonlinearities become proportionally greater. In the Dana Amplifier, AC linearity is better than 0.01% from DC through 2kHz as determined by the following equation:

$$\% \text{ Linearity} = 100 \frac{E_{out} - K E_{in}}{E_{out\,(\text{full scale})}}$$

High frequency linearity is measured with an extremely accurate ratiometer. Procedures for measurement are in Section 5, paragraph 5.4.5.

2.5 SLEWING SYMMETRY

It is commonly understood that nonlinear distortion will generate harmonics, second, third, fourth, etc., of the driving frequency. It is less commonly realized that a DC offset is also produced by nonlinear distortion. The Dana

Amplifier will be offset by less than 0.01% of full scale when driven up to 20 V peak-to-peak output, at any frequency from DC to 2 kHz. This offset will increase with frequency, but in a simple controlled manner to at least 20,000

This can be encountered as a practical problem when the amplifier must be used wideband to drive a magnetic tape recorder or other wideband load, and the amplifier output is also filtered and measured digitally.

At large amplitudes and frequencies beyond 20 kHz, a form of saturation may occur which is called "slew limiting" (see paragraph 2.9). Whenever this or any other saturation occurs, the offset is large and uncontrolled. The usefulness of data taken under these conditions is extremely questionable. If slew limiting is encountered, prefiltering is mandatory.

2.6 NOISE

Noise in a data amplifier is a complex function of bandwidth, gain, loop gain and other factors. The stabilization of large values of loop gain always produces a high degree of noise compared with open or low loop gain amplifiers, such as radar amplifiers. Excess noise is unavoidable, particularly in the higher frequencies near the limit of the bandwidth.

In addition to the inevitable random noise, there may be systemic noise at the line or chopper frequencies of their harmonics. In the Dana Amplifier, systemic noise is so nearly nonexistent as to be undetectable in the total noise except by very sensitive narrowband analyzers. Overall noise is random, but not uniformly weighted with respect to frequency.

Noise specifications are based on the total noise from an arbitrarily low-frequency (10-20 Hz) to the limit given. If less than the full amplifier bandwidth is specified, a single-pole, low-pass filter is assumed between the amplifier output and the noise-measuring instrument. The noise bandwidth is based on power transmission not voltage. The noise power bandwidth, in cycles per second, of a single-pole filter is (1/4 T) not (1/2 T) (conventional - 3dB point, where T = RC or L/R.

A true rms measurement is desirable, but the freedom from system noise makes reasonably accurate measurements possible with either an rms-calibrated average voltmeter or an oscilloscope (rms is approximately 1/6 the peak-to-peak value observed on the oscilloscope).

Noise on 1 kHz bandwidth is typically 1 uV rms. On wideband, peak noise is under 3 x rms spec 98% of the time.

2.7 CHOPPER INTERMODULATION

At signal frequencies harmonically related to the chopper in a chopper-stabilized amplifier, beat notes are produced. For example, at an (2 fc $\pm$ x) input, an x frequency output is produced by a "chopper intermodulation." The Dana Amplifier does not use a chopper of any type and thus does not require this type of specification.

2.8 BANDWIDTH (Applies to Model 2850 Only)

Bandwidth is one measure of an amplifier's ability to respond to rapidly changing signals. There are other measures, including rise time and settling time. Each measure has its application and is not interchangeable with the others.

Bandwidth in the Dana Amplifier is defined as the maximum frequency at which the gain remains within a specified tolerance from the DC gain. For example, from DC to 20kHz the amplifier will stay within $\pm$1 dB (within 89 to 112% of DC gain). At low amplitudes, the Dana Amplifier is flat to $\pm$3 dB to approximately 30 kHz on fixed gain steps, or at the low end of the adjustable gain settings.

The above refers to the basic non-restricted bandwidth of the amplifier. The bandwidth of "variband" units is -6 dB at the cutoff frequency $\pm$1 dB, decreasing at 18 dB/octave at higher frequencies.

Bandwidth is determined by observing the difference in AC gain at low and high frequencies. Procedures for measuring bandwidth are included in Section 5, paragraph 5.4.4.

2.9 SLEW LIMITING

All DC amplifiers, including the Dana unit, have a form of dynamic saturation called "slew limiting". The effect is to put a maximum limit on the rate-of-change of the output voltage, or dV/dt, and this in turn limits the peak voltage at a given frequency.

In certain cases, slew limiting may be due to an output current limit and a capacitive load so that $dV_O = I/C$. For example, if I = 10 ma and C = 0.02 uF, then dV_O/dt maximum = 500,000 volts/sec or a peak voltage of 4 volts at 20 kHz.

It should be noted that slew limiting may be the result of factors both internal and external to an amplifier. With no load the slewing rate of the Dana Amplifier is approximately 10^6 volts/second.

2.10 STEP-FUNCTION SETTLING TIME

Rise time specifications are of only limited use in digital systems since rise time indicates only when the signal passes within 10% of its final value for the first time. In digital work, a much longer period defined as settling time must be used. Settling time is measured to a small residual error, such as 0.1%.

2.11 OVERLOAD RECOVERY

From a 500% input overload of any duration, the Dana Amplifier recovers to final value $\pm$0.1% of full scale within 2 milliseconds. With an input overload of 10 volts, recovery to final value, $\pm$0.1% of full scale, $\pm$10 uV referred to input occurs within 10 milliseconds. No damage will be sustained from input overloads of 30 volts DC or peak AC.

2.12 COMMON MODE REJECTION (CMR)

At DC and very low frequencies, amplifiers of any type basically respond to the electrical "difference" between two points and do not respond to potentials between these two points and a third point, such as a specific earth ground (common mode potential). The fact that two types of amplifiers can yield two difference results when connected alternately to a given pair of signal lines can only be attributed to the fact that once connected, the new current paths introduced by the amplifier cause new and undesirable "difference" voltages to be developed which constitute an actual input signal. These new "difference" potentials common to both input lines. If the impedances involved are perfectly symmetrical, the sum of the IR drops equal zero and no difference signal will be seen. Similarly, if the common potential is open circuited, no current can flow and no difference signal will be developed. Since it is seldom practical to balance the complete input system (including the amplifier) the only alternative is to raise the effective common mode impedance of the circuit, reducing undesirable currents to a minimum. For this reason, simple Common Mode Rejection specifications are meaningless unless fully defined in terms of impedance.

Figure 2 shows a balanced differential amplifier specified to have a common mode rejection of 100 dB. Operating in a practical circuit with 100 ohms of resistive unbalance and a common mode potential of 1 volt, it can be readily seen that the actual rejection is far less than 100 dB.

In addition to illustrating the importance of common mode impedances insofar as the amplifier is concerned, the diagram in Figure 2 can be altered to show that the same degradation can occur without an amplifier. To illustrate, mentally reposition the 50 k resistors outside of the amplifier to represent the cable capacity of an improperly driven cable (approximately 500 ft. of 100 μμF/ft. at 60 Hz). Under these circumstances, the amplifier cannot possibly break the circulating currents and even with a perfect amplifier the system common mode rejection would be only 43 dB.

The Dana Amplifier is similar to the unit shown in Figure 2 in that the input is nearly symmetrical; however, the effective impedance seen by each input line is greater than 350 megohms at DC through 60 Hz. With this high impedance, common mode rejection is 120 dB with up to 350 ohms of input unbalance.

2.13 SYSTEM COMMON MODE REJECTION

As previously noted, improper system connections can allow common mode currents to flow through source impedances and develop undesirable "difference" potentials that appear as normal mode signals to the amplifier. A typical example of improper cable management is shown in Figure 3. In this diagram, the common mode voltage sees a complete circuit through the source resistor and cable capacity to ground at the amplifier site. Note that the amplifier's effective impedance to ground is in parallel with the cable capacity. This again illustrates that even with infinite isolation, the amplifier cannot control external current paths and considerable care must be exercised in designing the system or the fine isolation of the amplifier will be wasted. To further illustrate the importance of great care, it should be noted that one inch of cable (100 pF/foot) is

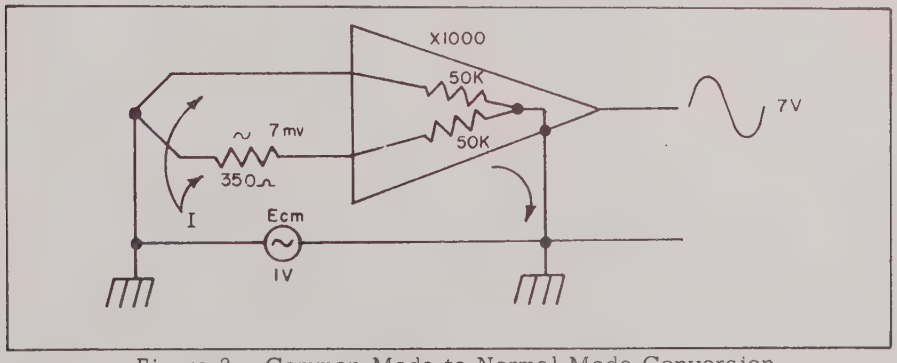


Figure 2 - Common Mode to Normal Mode Conversion

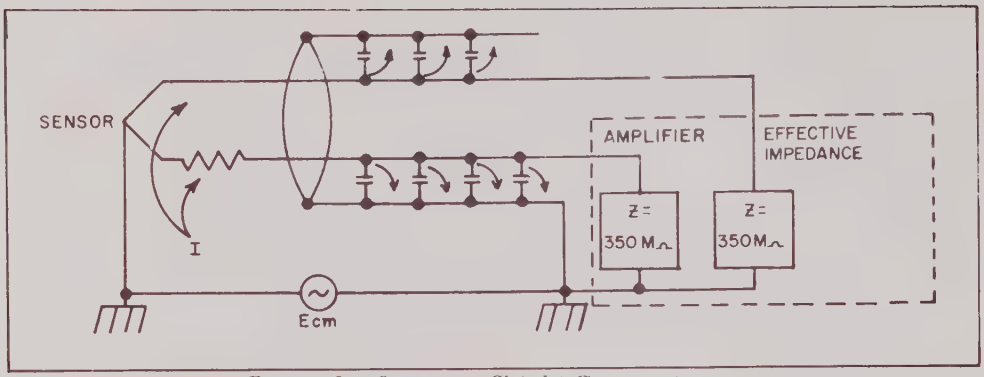


Figure 3 - Improper Shield Connections

approximately 350 megohms at 60 Hz — equal to the Common Mode impedance of the amplifier.

Figure 4 shows a properly guarded system with the shield being driven at the common mode voltage. This almost eliminates the effective capacity between the signal lines and the measurement site ground, sharply reducing common mode currents through the source resistance. Currents that do flow will pass harmlessly through the guard shield. Unfortunately, it is normally impossible to drive the guard at the precise Common Mode Voltage; therefore, the cable capacity cannot be completely neutralized. Furthermore, pinholes in the cable, together with exposed wiring in patch panels, terminal strips, etc., typically combine to produce an effective impedance between each input line and ground of less than 10 megohms at 60 Hz. Since shunting this impedance with the 350 megohms of the Dana Amplifier would obviously produce very little change, it becomes quite clear that the total CMR of the system is essentially determined by the system itself, not the amplifier. Practically speaking, a well designed system will have a maximum CMR of 90 to 100 dB with typical source unbalances. This renders the CMR of the amplifier virtually academic above 110 or 120 dB.

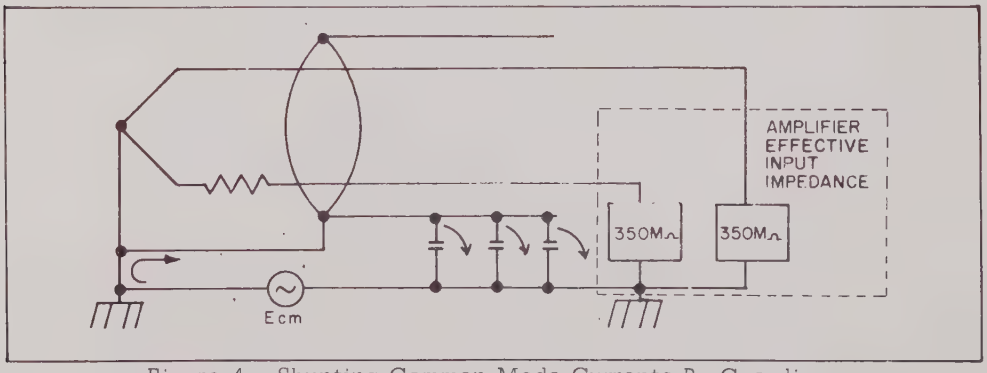


Figure 4 - Shunting Common Mode Currents By Guarding

Full comprehension of the above limitations introduces a second important consideration into the design of the system, control of the magnitude of the Common Mode potential. To illustrate, consider a system with the following design objectives:

1. Full scale 0 to 10 millivolts
2. Accuracy .25% (exclusive of transducer and recorder)

Assuming that the system will have a CMR of 100 dB (not a minor design objective) and that .1% of the accuracy tolerance can be allotted to common mode components in the output signal, the total error voltage (CM voltage converted to difference voltage) at the amplifier's input terminals cannot exceed 10 microvolts. This limits the total common mode voltage to 1 volt ($1V/10^5 = 10\,\mu V$). In the event a system CMR of 100 dB cannot be realized, the maximum CM voltage is even lower.

Control of Common Mode voltage varies in complexity as a function of local conditions. In many instances no specific action is necessary or a simple bus wire may be required between sites. In other cases, efforts such as strapping structural members, balancing three-phase loads to neutral, line filters installed on interference generating devices, etc., must be pursued.

2.14 INPUT IMPEDANCE

The input impedance is essentially a stable, passive 10-megohm DC resistance. Capacity shunt effects are allowed for in the frequency response and source impedance specifications.

The amplifiers are designed specially to be operated from low level transducers such as thermocouples and strain gages. The 10 megohms will cause a loading error of 0.0035% when operated from a 350-ohm strain gage. Even this minute error is absorbed by normal strain gage calibration procedures. Thermocouples usually have even lower internal resistances. Operation from higher source impedances is possible with some degradation in performance characteristics.

2.15 ZERO DRIFT

Characteristically, zero drift is the greatest single error in data amplifiers. This drift has no effect on frequency response, linearity, and other parameters, but merely displaces the output. There are two components of drift, voltage and current. The voltage component of drift can be measured if the input is shorted, or if operation is from transducers of such low resistance as to make negligible the effect of current drift.

The Dana Amplifier drift specification, based on a fixed 0-350 ohm signal source, is $\pm 0.02\%$ of full scale, or ± 2 mV referred to the output in 200 hours. This is ± 2 microvolts referred to the input when the gain is set to X 1000.

In addition, the temperature coefficient specification is $\pm$0.001% of full scale and $\pm$1 µV referred to the input, per-degree-centigrade temperature change. This totals $\pm$1.1 µV/per ^{o}C referred to the input at K = 1000. Since this also includes the source unbalance, both voltage and current errors are summed.

2.16 OFFSET CURRENT

A portion of the zero drift is due to an IR drop in the transducer. Resistance is normal to DC output type transducers, and all DC amplifiers produce some offset current through the transducer. In the Dana Amplifier, the offset current is typically less than 5×10^{-9} amperes from each input, returning through the transducer to common at 25^{o}C. This may change approximately $\pm 10^{-9}$ amperes per degree centigrade. The Dana Amplifier drift specification is based upon a maximum fixed source resistance of 350 ohms and includes the change in the IR drop. Higher resistance transducers may produce larger than specified drift/temperature coefficient because of this effect.

Dana Laboratories hopes that this Appendix has helped you to understand the nature of the Dana Data Amplifiers, and will help you to put the Dana Amplifier to the most effective use in your application.

Warranty

It is the practice of Dana Laboratories, Incorporated, to manufacture only products of a quality that will merit customer satisfaction. The company recognizes that customer satisfaction is achieved, not only by delivering products meeting advertised performance specifications and having a high level of reliability, but also by honestly and efficiently fulfilling their warranty obligations as set forth below.

Dana Laboratories, Inc., agrees to correct, either by repair or replacement, any defect of material or workmanship in Dana-manufactured units or components which develop within one year after delivery of the equipment to the original purchaser — provided that the equipment has been subjected only to normal and proper use.

In the event of failure of any component delivered with Dana equipment, but not manufactured by Dana Laboratories, assistance will be given the customer in obtaining, from the original manufacturer, reasonable adjustment under that manufacturer's warranty.

Any item claimed to be defective during the warranty period must be returned to Dana Laboratories, Inc., with transportation charges prepaid. The item will be repaired and returned to the purchaser with return transportation prepaid by Dana unless, of course, the item is found not to be defective or found to be damaged by misuse — in which case it will be returned to the purchaser with repair and transportation billed collect.

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